SDL-9-588

ELECTRONIC INSTABILITIES IN METAL-INSULATOR-SEMICONDUCTOR DEVICES

NASA GRANT NsG-588

Theoretical and Experimental Studies of Radiation Damage to Semiconductor Surfaces and the Effects of this Damage on Semiconductor Device Performance

1 September 1968

by

J. R. Hauser
J. R. Bridges

Semiconductor Device Laboratory
Department of Electrical Engineering
North Carolina State University
at
Raleigh, North Carolina

ABSTRACT

This report discusses instabilities in metal-insulator-semiconductor devices with special emphasis on the electronic type of instability present in silicon nitride MIS devices. In general, instabilities in MIS devices can be classified as ionic or electronic in nature. Ionic instabilities arise from ion transport within the insulating film while electronic instabilities involve the flow of electrons and holes from the semiconductor to trapped states either at the semiconductor-insulator interface or within the bulk of the insulator.

A model is presented and discussed for electron and hole injection from the semiconductor into the insulator over a Schottky barrier, with the subsequent trapping of the carriers within the insulator. For a step bias voltage applied to an MIS device this is shown to lead to an injected charge within the insulator which depends on time as approximately ln(t) for many orders of magnitude in time following some initial time interval. For low insulator energy band gaps, this leads to a very pronounced and long time instability which causes a shift in the C-V characteristic which is opposite to that of an ionic instability.

Experimental results are presented for the instability present in silicon nitride devices, and this is shown to be in reasonably good agreement with the Schottky barrier injection model. The energy band gap for the silicon nitride films obtained from the charge instability measurements is 4.2ev $\pm$ 0.2ev.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (cont'd)

1. INTRODUCTION

Probably the most pronounced factor which has so far limited the wide-scale use of metal-insulator-semiconductor (MIS) devices in electronic equipment is the charge instabilities which have been found to be associated with the insulator layer. The most extensively investigated system is that in which the insulator is thermally grown SiO_2 either by a steam oxidation or a dry oxygen oxidation [1]. The major type of instability in SiO_2 has been identified as ion motion in the oxide under applied electric fields [2], [3], [4], [5], [6]. Sodium ions incorporated into the oxide during the growth process or metalization process has been shown to be the most likely cause of the instability. Great strides have been made in the past few years in eliminating ions from oxide layers by the use of ultra clean techniques in the manufacturing process. This has made it possible to produce metal-oxide-semiconductor devices which are relatively stable at temperatures up to 300°C [7].

In attempts to overcome some of the limitations of SiO_2 insulator layers, other materials have been the subject of detailed investigations in recent months. Two of these are silicon nitride (Si_3N_4) and aluminum oxide (Al_2O_3). While ion migration can be greatly reduced in these materials [8], [9], [10], [11], they have so far exhibited a different type of instability in which electronic charge is transfered or injected from the semiconductor or metal into the insulator where it becomes subsequently trapped [12], [13]. This build-up of trapped charge, either electrons or holes, in the insulator causes a shift of the electrical characteristics with time of these devices. This instability is especially pronounced in Si_3N_4 devices where rapid room temperature shifts in the flat band voltage of MIS capacitors occur.

The present work is devoted to a discussion of this electronic charge injection instability as opposed to the ionic instability which has been extensively investigated in connection with SiO_2 insulating layers. A model is presented for the electronic instability which is based on electron and hole injection between the electrodes (metal or semiconductor) and the semiconductor over a Schottky barrier. A comparison of the model with experimental data on Si_3N_4 devices is also presented.

The present investigation arose from initial work on radiation effects on Si_3N_4 layers [12]. Early work under the present contract investigated the effects of gamma radiation on thermally oxidized silicon wafers [14], [15]. The effects of radiation on oxide charge build up as well as the effects on surface and bulk recombination were studied and reported in previous reports [15], [16]. Because of the increased interest in Si_3N_4 films as insulating layers in recent years, it appeared to be desirable to investigate the differences in radiation effects on SiO_2 and Si_3N_4. When initial attempts were made to study gamma radiation effects on nitride films, these effects were found to be masked by the electronic instabilities present in the nitride devices. From this work it became apparent that useful radiation effect results could not be obtained with the large electronic instabilities present in the nitride films. This led to the present work which is concerned with the physical origin of the electronic instabilities present in the nitride films.

In a previous report, two models were suggested for the instabilities present in nitride devices [12]. One of these is charge injection from the electrodes (both the silicon and metal) into the nitride films. This can be injection either over the energy barrier between the electrodes

and the insulator, i.e. Schottky barrier injection, or tunneling into the conduction band of the nitride film from the electrodes, i.e. Fowler-Nordheim emission. The present experimental data indicates that Schottky barrier injection of both electrons and holes is probably the dominant process.

2. INSTABILITIES IN METAL-INSULATOR-SEMICONDUCTOR DEVICES

This chapter contains a discussion of the various types of instabilities which can occur in MIS structures and how these affect the electrical properties of devices. The term instabilities is used here to refer to time dependent changes in the electrical properties of a metal-insulator-semiconductor device which are not predicted by the ideal metal-insulator-semiconductor model. The ideal MIS model is assumed to be that of a perfect insulator with no electronic states in the insulator or at the interface between the insulator and semiconductor. This is just the model normally used in analyzing MIS capacitors. Within this definition of instabilities then, interface states of either the fast or slow type give rise to time dependent effects which are classified as instabilities. Other types of instabilities arise from charge motion in the insulator layer. In many cases it is difficult to experimentally distinguish between bulk insulator charge effects and interface states. This is particularily true with the electronic type of instability which is discussed in detail in this report.

The energy band diagram for an ideal MIS device is shown in Figure 1. A difference in work function between the metal and semiconductor results in a small amount of band bending in the insulator and semiconductor. The ideal MIS device has been analyzed in great detail by many investigators [1], [17], [18], and the ideal C-V characteristic for such a device with an n-type semiconductor is shown in Figure 2, where V is the metal-to-semiconductor voltage. The flat band capacitance C_{FB} is an important point on the C-V curve and this occurs at V=0 for the ideal MIS device with equal metal and semiconductor work functions. The value of flat band capacitance per unit area is given approximately

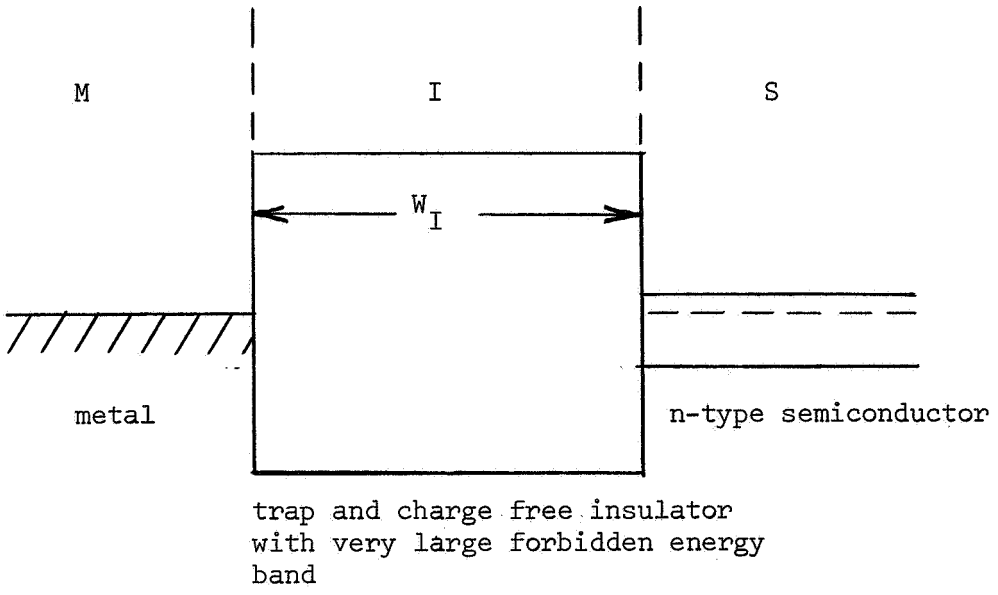


Figure 1. Energy band diagram for an ideal MIS device

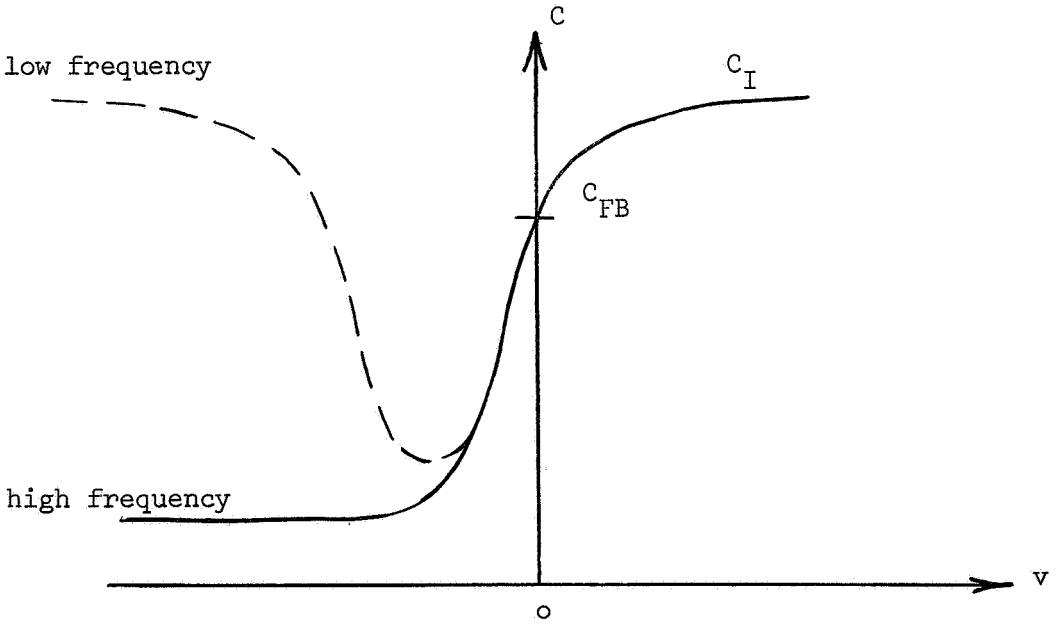


Figure 2. C-V characteristic for ideal MIS device (n-type semiconductor)

by the expression [19]

$$C_{FB} = \frac{C_I \, C_{SFB}}{C_I + C_{SFB}} \quad , \tag{1}$$

where

$$C_{SFB} = q(\varepsilon N_D/kT)^{1/2} \quad , \tag{2}$$

and C_I is the ideal insulator capacitance per unit area given by

$$C_I = \frac{\varepsilon}{W_I} \quad . \tag{3}$$

N_D is the bulk impurity density in the n-type semiconductor. The flat band capacitance is the MIS capacitance when the semiconductor energy band is flat at the surface, or when the electric field at the interface is zero. This value of capacitance is of significance even for non-ideal MIS devices.

Practical MIS structures are modified in several significant ways from the ideal structure. These changes arise from the non-ideal nature of practical insulator layers. For the purpose of this discussion the electronic energy levels in the insulator will be discussed in semiconductor terms, i.e. the insulator is assumed to be a wide band-gap semiconductor. There is certainly some question as to the validity of carrying over completely all semiconductor concepts to insulators, especially amorphous insulators such as Si_3N_4. Because of the lack of a nice crystal structure in these materials, electronic motion may be due more to a hopping mechanism than to a band conduction mechanism. Certainly if the insulator mobility is low ($< 1 cm^2/v$ sec) such a possibility must be seriously considered. In terms of a model for the insulator, however, charge carrier transport by hopping is very similar to an energy band model with traps. The important features of both models

are the existence of high energy levels in which the electron can be transported through the insulator, and the existance of lower energy levels at which the charge carrier is no longer free to move within the insulator. The insulator energy band model assumed, then, is that of a wide band-gap semiconductor with traps for both electrons and holes.

There may also be additional electronic energy levels in the insulator forbidden band due to impurities within the insulator. These will give rise to donor like or acceptor like states depending on whether the impurity is more likely to give up an electron or capture an electron. Both electron trap sites and donor like impurity sites can be occupied by electrons. The distinction however is that electron trap sites are charged negatively when occupied by an electron while donor sites are neutral when occupied by an electron and positively charged when unoccupied by an electron.

An additional complication present with insulators and not normally encountered with semiconductors is the fact that ionized impurity atoms in the insulator can move under the influence of the large electric fields which are normally applied to MIS devices. Sodium ions are examples of espically troublesome ions because of their large mobility.

The energy band diagram used for a non-ideal insulator in this work is shown in Figure 3. The electronic levels within the forbidden band are shown in Figure 3 as discrete energy levels. This is for convenience only, and in most insulators the levels are likely spread into an energy range or even over the entire energy band. The densities of traps and impurities may also be spatially dependent upon distance within the insulating layer.

Certainly in SiO_2 the ion density is spatially dependent, and there is strong experimental evidence to indicate that the trap density is greatest near the insulator boundaries. This is to be expected if the defect density is largest near the interfaces. Similar effects are also probably to be expected with Si_3N_4. Also sketched in Figure 3 are interface states located at the insulator-semiconductor interface.

In equilibrium the net effect of the above mentioned non-ideal insulator properties is to give rise to a non-zero net charge within the insulator. In principle this can be either positive or negative, but for SiO_2 and Si_3N_4 it is experimentally found to be positive. Part of this for SiO_2 is known to be due the presence of ions such as sodium. However even when sodium ions are reduced to a minimum there still remains a fairly immobile positive charge in SiO_2 near the silicon interface. Silicon ions have been suggested as the origin of

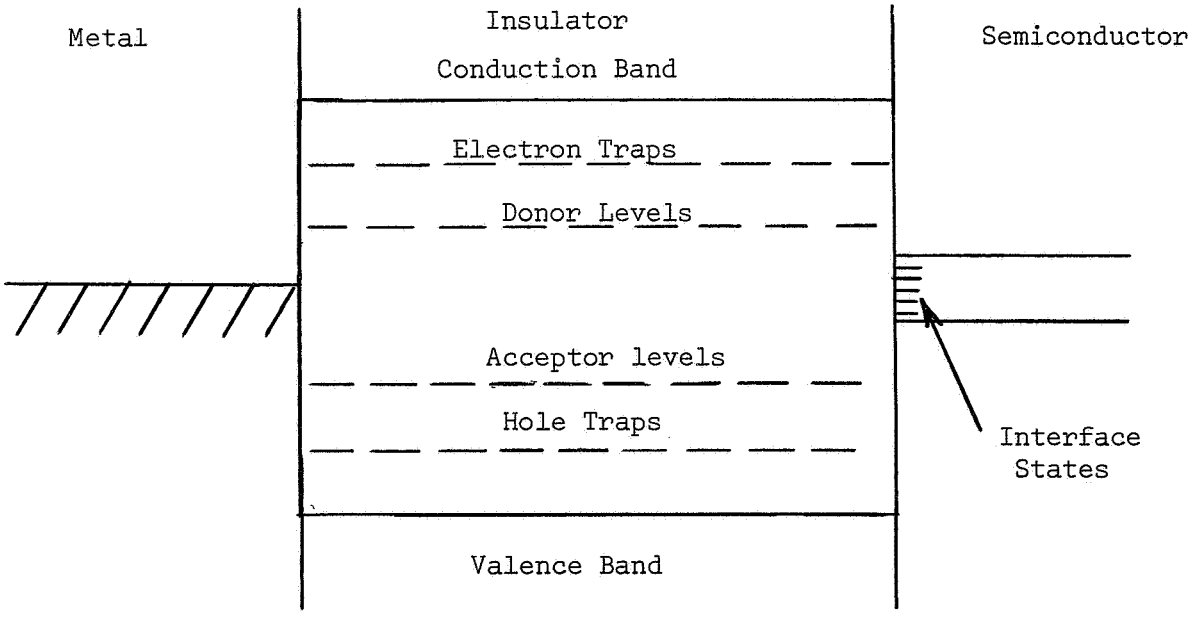


Figure 3. Energy band diagram for a non-ideal insulator. (Discrete levels shown for convenience only)

this charge [20]. For Si_3N_4 and other insulators the exact origin of the charge is more in question, but experimentally, positive values of net equilibrium charge are found. Donor like impurities within the insulator can give rise to a net positive charge as shown in Figure 4, and if the donor like impurities are located near the metal-insulator or semiconductor-insulator interfaces, essentially all of them can become ionized.

An MIS device with a non-ideal insulator has its electrical properties modified in several important ways from that of the ideal device. There are several ways in which the C-V characteristic for example can be modified. Consider first the case of a fixed immobile charge within the insulator which does not change from its equilibrium value. This is known to give rise to a parallel shift of the ideal capacitance curve, as sketched in Figure 2, along the voltage axis [17]. This is shown in Figure 5. Positive and negative insulator charges cause shifts in opposite directions.

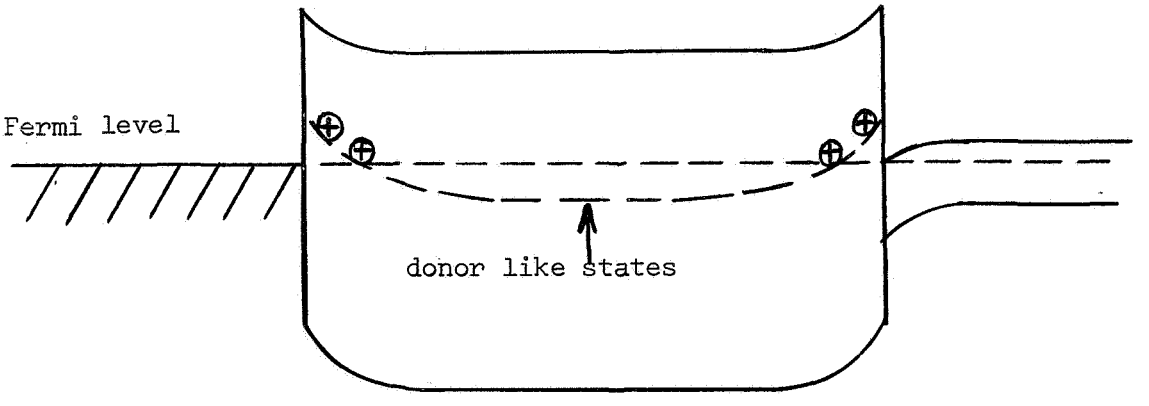


Figure 4. Net positive insulator charge due to donor like insulator Impurities

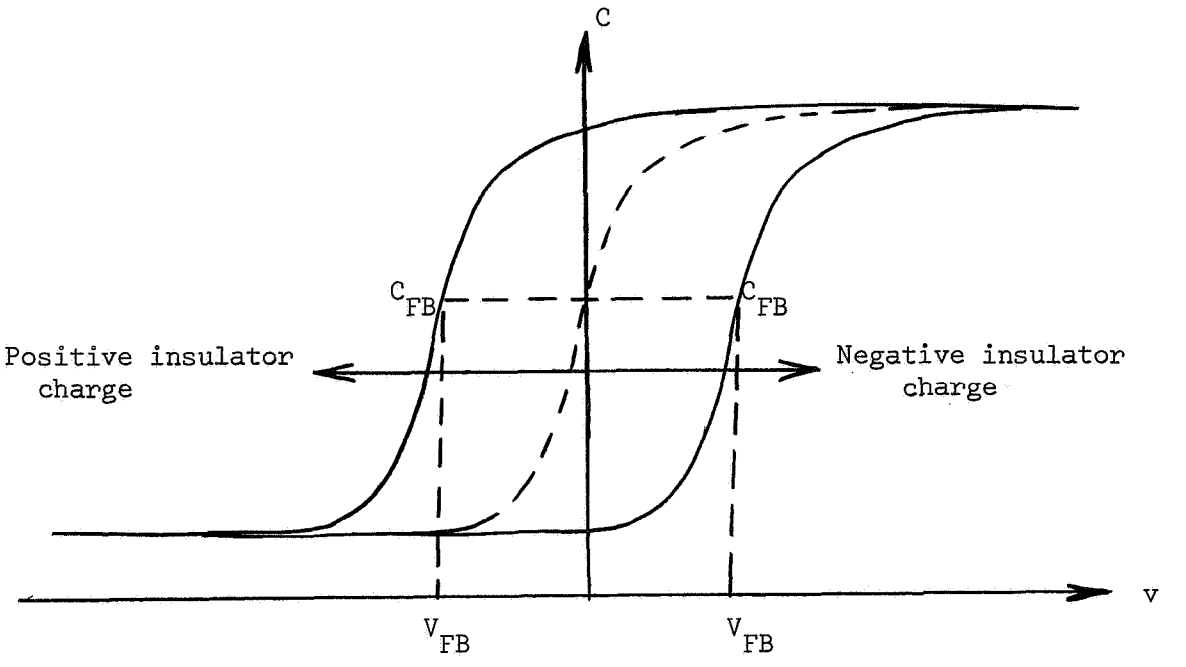


Figure 5. C-V characteristic of an MIS device with a fixed insulator charge. (n-type semiconductor)

The voltage at which the flat-band capacitance occurs, or the flat-band voltage V_{FB}, is still an important parameter. At this value of applied voltage the electric field at the semiconductor-insulator interface is zero and the field lines from the metal electrode are just sufficient to terminate on all the charges in the insulator. The flat-band voltage is related to the charges in the insulator and surface states by the expression [17]

$$V_{FB} = \phi_{ms} - \frac{Q_{ss}}{C_I} - \frac{1}{C_I} \int_o^L \frac{x}{L} \rho(x)dx, \qquad (4)$$

where ϕ_{ms} is the metal-to-semiconductor work function difference, Q_{ss} is the surface state charge located at the semiconductor interface, and $\rho(x)$ is the charge density within the insulator. The flat-band voltage then provides a measure of the charges associated with the non-ideal insulator. A limitation of the flat-band voltage measurement is the fact that it indicates only the right hand side of Equation (4) and does not permit one to separate out bulk insulator effects from surface state effects.

Bulk insulator charge densities have been obtained in some cases by combining C-V measurements with successive etchings of the oxide. In this way L, the insulator thickness, is changed, and by measuring V_{FB} as a function of L, $\rho(x)$ can be determined.

It is possible to define the flat-band voltage in terms of a single effective surface state charge Q_s in the following manner:

$$V_{FB} = - \frac{Q_s}{C_I} \tag{5}$$

where

$$Q_s = Q_{ss} + \int_o^L \frac{x}{L} \rho(x)dx - \phi_{ms} C_I \tag{6}$$

This effective charge has the significance of being the charge which if placed at the insulator-semiconductor interface would cause the same shift in the C-V characteristic as that produced in a real case by the combined effects of work-function difference, surface state charge, and bulk insulator charge.

Another complication arises with real insulators in the fact that the surface state and even insulator charge is rarely constant but changes with applied bias. This is never an instantaneous process, so one also observes time dependent effects. The exact shape and position of the C-V curve in general depends on the past bias history of the structure as well as on the rate at which the C-V curve is observed. These bias and time dependent effects on surface state and insulator charges make for an infinite variety of observed C-V curves depending on how the C-V curve is obtained. Some of the possible cases of bias dependent surface state and insulator charges and the effects of these changing charge densities on C-V curves are discussed in the following paragraphs.

Consider first the manner in which C-V curves such as shown in Figure 5 are experimentally obtained. These are normally obtained by slowly changing the bias across an MIS structure and measuring with a bridge the capacitance of the structure. The capacitance measurement requires a small signal, high frequency voltage across the device superimposed on the slowly varying bias voltage. Typical frequencies for the small signal voltage are 100 kHz or 1 MHz. By a slowly changing bias voltage then we mean a bias voltage which changes slowly enough to permit many cycles of the ac voltage while the capacitance changes only a small percentage of its total change. As an example, suppose the maximum-to-minimum capacitance change in Figure 5 occurs with a bias voltage change of 1 volt. Further, suppose that 10^2 is set as the minmum number of cycles of ac signal desired during this interval in order to measure the capacitance. Then for a 100 kHz ac signal, the bias sweep on the device voltage must be at a rate greater than 10^{-3} sec/volt. For a total voltage change of 50 volts, the slowly changing bias must then take 50 m sec or longer to complete the C-V curve. If one uses a 1 MHz ac signal the minimum sweep time (for a 50 volt sweep) can be 5 m sec. These considerations yield maximum rates at which the C-V curve can be observed for a device. On the other end of the scale the bias voltage may be changed as slowly as possible, so that one approach steady state conditions at any given bias voltage. As previously noted, when the surface state and insulator charges are bias and time dependent, the observed C-V curve is greatly influenced by the rate at which the bias voltage is changed.

From Gauss' law and the definition of capacitance, it can be shown that the MIS capacitance for the non-ideal insulator is [21]

$$C_j = \frac{\frac{dQ_{sc}}{d\psi_s} + \frac{dQ_s}{d\psi_s}}{1 + \frac{dQ_{sc}}{d\psi_s} + \frac{dQ_s}{d\psi_s}} , \tag{7}$$

where Q_{sc} is the charge located in the semiconductor (in an accumulation layer, or in a depletion and inversion layer) and ψ_s is the potential in the semiconductor at the insulator-semiconductor interface. By defining the following voltages

$$\begin{aligned} V_{sc} &= \frac{Q_{sc}}{C_I} , \\ V_s &= \frac{Q_s}{C_I} , \end{aligned} \tag{8}$$

the above equation can be written as

$$C = C_I \frac{\frac{dV_{sc}}{d\psi_s} + \frac{dV_s}{d\psi_s}}{1 + \frac{dV_{sc}}{d\psi_s} + \frac{dV_s}{d\psi_s}} . \tag{9}$$

The quantity $dV_{sc}/d\psi_s$ can be theoretically evaluated under certain assumptions by applying Poisson's equation to the semiconductor, so this can be considered as a known function of ψ_s [21].

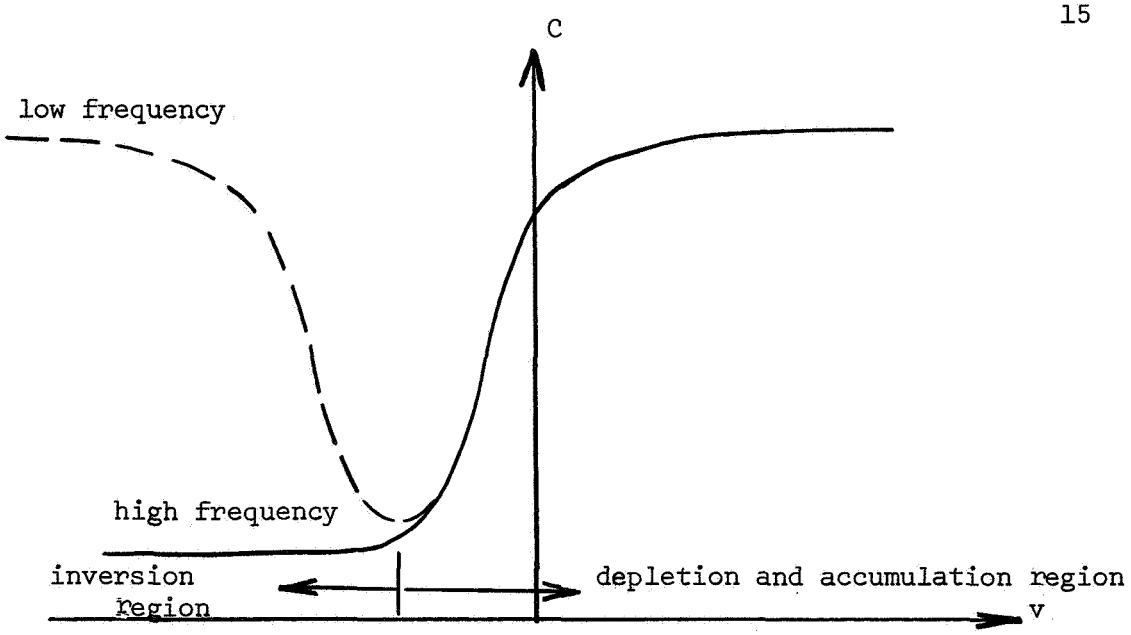
The quantity $dV_s/d\psi_s = C_I^{-1} dQ_s/d\psi_s$ represents the contribution of the surface state and insulator charge to the measured capacitance. The change in ψ_s under consideration in this equation is the change due to the small ac voltage used in measuring the capacitance. There will always be a certain delay between a changing surface potential and any response in the surface state and insulator charge. For surface states, the response time is the trapping time or release time of the localized states. If the frequency of the small signal ac voltage is high enough, the surface state and insulator charge will not be able to change

significantly during a half cycle of the ac voltage. Under these conditions $dV_s/d\psi_s$ will be very small and can be neglected in Equation (9). This reduces Equation (9) to the form

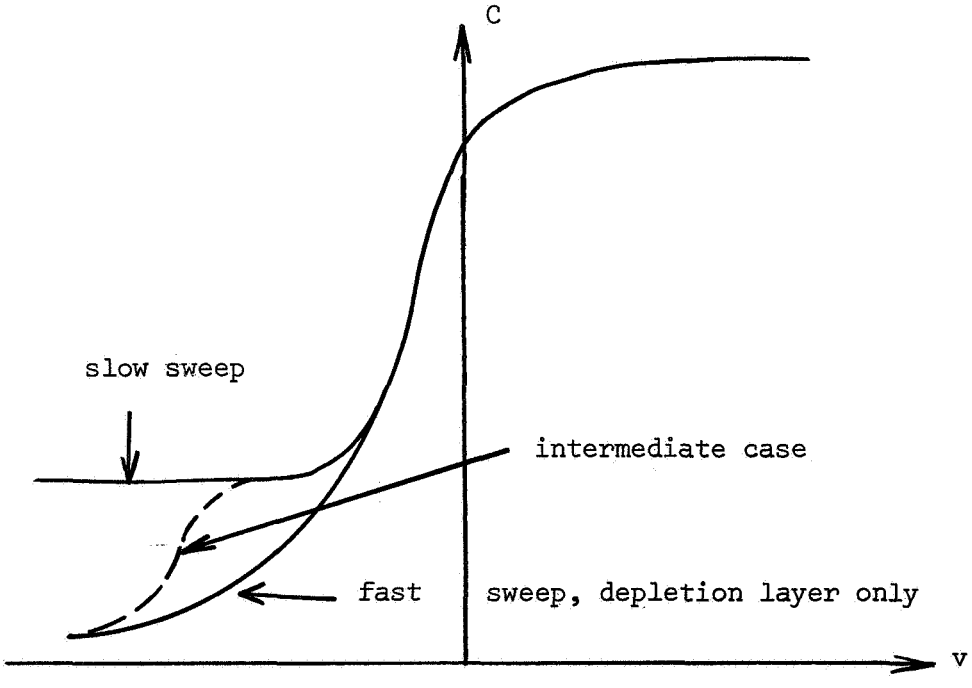
$$C = C_I \frac{\frac{dV_{sc}}{d\psi_s}}{1 + \frac{dV_{sc}}{d\psi_s}} . \qquad (10)$$

The frequency at which the term $dV_s/d\psi_s$ becomes negligable can be determined experimentally by observing the C-V curve for various frequencies and determining the frequency above which the curve remains constant.

There is also a time response on $dV_{sc}/d\psi_s$, i.e. there is a delay between a surface potential charge and the response of the charges in the semiconductor surface space charge layer. For majority carriers the response time constant is the dielectric relaxation time which is normally very short compared with the time of interest in MIS devices. Thus for all practical purposes, majority carriers respond instantaneously to a change in surface potential. For minority carriers, however, the response time constant is that for the generation or recombination of excess carriers. Normally for frequencies somewhere above 100Hz, the minority carriers are not able to respond to the rapid changes in potential. In the accumulation and depletion regions of an MIS capacitor the majority carriers make the major contributions to the capacitance, and one observes an ideal capacitance which is independent of frequency. When the bias voltage is such that an inversion layer is established, one has both majority and minority carrier contributions to the capacitance. This leads to the well-known difference between the low frequency and high frequency theoretical MIS capacitance curves [17], [18] as shown in Figure 6a for a very slow bias sweep.



(a) Low and high frequency curves for slow bias sweep rate.



(b) Effect of bias sweep speed on ideal high frequency curve

Figure 6. Ideal C-V curve for MIS devices

The bias sweep rate also affects the ideal C-V curve as illustrated in Figure 6b for the high frequency ac case. As with the high and low frequency ac signal, the region of the C-V curve which is affected by the bias sweep rate corresponds to the inversion space charge layer region in the semiconductor. For a fast bias sweep rate, the minority carriers are not able to equilibrate during the sweep time. Consequently the inversion layer does not have sufficient time to form and only a wide non-equilibrium depletion region exists. For this case, the negative bias capacitance is considerably less than the measured capacitance when sufficient time is allowed for the minority carriers to equilibrate and form the inversion layer. Intermediate bias sweep rates can result in composite curves such as the curve shown dashed in Figure 6b. In the experimental work reported herein, all three types of C-V curves shown in Figure 6b have been observed on different silicon nitride MIS devices.

The above discussion has illustrated the effects which ac frequency and bias sweep rate can have on the ideal C-V curve for an MIS device. Fortunately for extracting useful data from C-V measurements, the ideal C-V curve in the depletion and accumulation regions are not effected by the signal frequency or bias sweep rate. Thus the flat-band voltage remains a measure of the surface state and insulator charge independent of the signal frequency and bias sweep rate. In the depletion and accumulation regions of the C-V curve the capacitance is then a unique function of surface potential, i.e.

$$C = C_I \frac{\frac{dV_{sc}}{d\psi_s}}{1 + \frac{dV_{sc}}{d\psi_s}} = C(\psi_s). \tag{11}$$

This means that at the instant one observes the flat-band capacitance on any C-V curve, the corresponding value of flat-band voltage has the value

$$V_{FB} = \phi_{ms} - \frac{Q_{ss}}{C_I} - \frac{1}{C_I} \int_o^L \frac{x}{L} \rho(x)dx, \tag{4}$$

This is true regardless of whether Q_{ss} and $\rho(x)$ are time dependent.

The ideal MIS capacitance has now been discussed in detail as well as the effect of a fixed surface state and oxide charge which results in a parallel shift of the ideal curve along the voltage axis. To complete the discussion, the effects of bias dependent and consequently time dependent surface state and oxide charges must be considered. In this discussion it will be assumed that a high frequency ac signal is used so that the surface state and insulator charges cannot respond to the ac voltage. As discussed above, this makes the capacitance a unique function of the surface potential in the depletion and accumulation regions. Consequently, any difference between the ideal MIS capacitance and an actual measured C-V curve must arise from the surface state and oxide charge which modifies the surface potential for a given applied bias voltage.

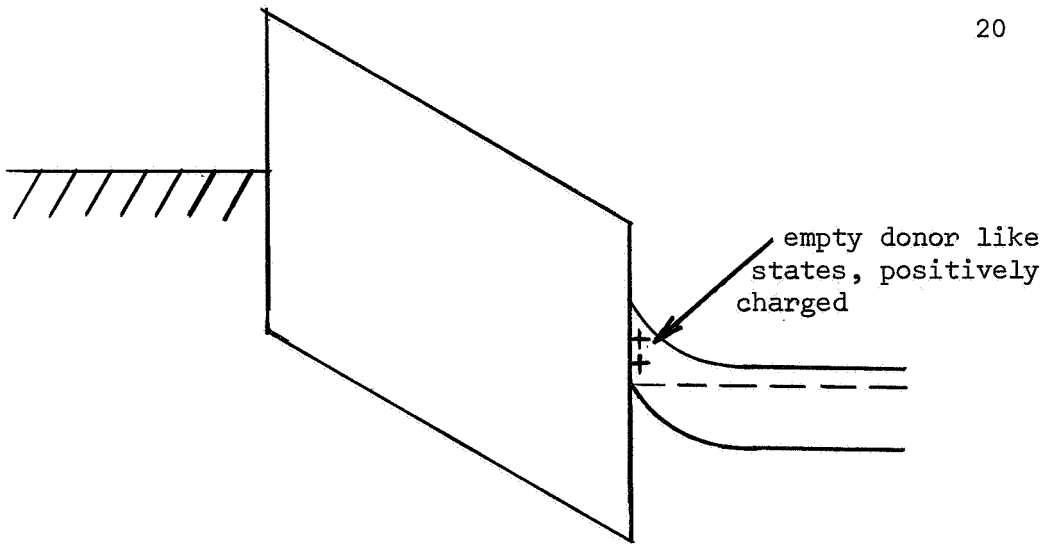
Using a high frequency ac voltage, one still has the liberty of using either a slow or fast bias sweep in observing the C-V characteristic. Both techniques can be used to extract information concerning the surface state and insulator charges. As discussed earlier any bias dependent surface state and insulator charges do not change instantaneously but require some time to equilibrate after a bias voltage change. If the bias sweep occurs at a fast enough rate, these charges will change very little

during the period of the high frequency ac voltage. Then for a very fast sweep rate, the flat-band voltage will give a measure of the surface state and insulator charge at the start of the C-V trace. At any given instant of time then, one can investigate the surface state and insulator charge by making a fast bias sweep C-V measurement and noting the flat band voltage. On the other hand for a very slow C-V bias sweep the charges in surface states and in the insulator have time to reach equilibrium at any given bias voltage and the surface state and insulator charge state changes as the C-V curve is measured. For a fast bias sweep one observes a fixed charge and simply a parallel shift of the ideal C-V curve along the voltage axis. For a slow bias sweep one observes a distortion in the ideal C-V curve as well as a possible displacement along the voltage axis. The slow bias sweep condition is the case which has most frequently been used in studying MIS devices, especially silicon oxide devices. In the present work on silicon nitride devices fast bias sweep C-V curves have been found to be more useful in studying the instabilities or time changing charges present in these devices.

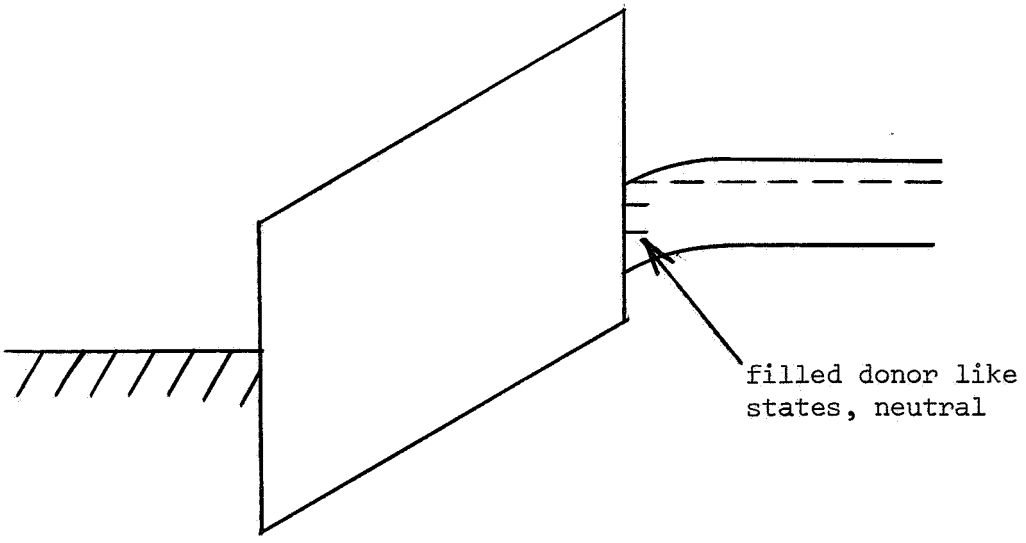
It is apparent from the above discussion, that the terms fast bias sweep and slow bias sweep are relative terms depending on the time constant associated with the bias dependent charge mechanism. In fact one can have a bias sweep rate which is slow with respect to changes in surface state charges but fast with respect to changes in the insulator charges. This is the case normally encountered with silicon oxide charges. In this case one sees a distortion of the C-V curve due to surface states and a shift along the voltage axis due to the oxide charge. With silicon nitride as an insulator, the bulk insulator charge changes much faster than for silicon dioxide, so a considerably faster bias sweep is required to have a fast bias sweep with respect to bulk insulator changes.

There are several different types of instabilities or time dependent charge changes which can occur with MIS devices. These are discussed and compared in the following paragraphs.

Consider first the case of bias dependent surface states with zero or constant insulator charge. Bias dependent surface state charge can arise from either donor like or acceptor like states at the surface within the forbidden band. The energy band diagrams for donor like surface states under large positive and negative bias voltages are shown in Figure 7. For a large negative voltage, the donor like states are unoccupied and the surface states are positively charged, while for a large positive voltage the sites are occupied by electrons and are electrically neutral. Consider a very slow bias sweep, C-V curve for such a situation starting from a large negative voltage. The C-V curve will start out as an ideal C-V curve displaced along the voltage axis because of the positive charge of the empty surface donor sites. The surface states will remain unfilled until the surface potential has changed to the point where the Fermi level at the surface is within a few kT of the assumed discrete level. The surface states then begin to fill with electrons, and they become essentially all filled when the surface Fermi level is a few kT above the surface state energy. Thus the donor like surface states go from a large positive charge state to an electrically neutral state while the surface potential changes by a few kT. Since the capacitance is a unique function of the surface potential there is little change in the measured capacitance during the time while the surface states are becoming filled. On the other hand a large change in applied bias voltage is required to go from the charged to the uncharged state of the surface states. The required bias voltage change is



(a) Large negative bias



(b) Large positive bias

Figure 7. Energy band diagrams for MIS device with donor like surface states.

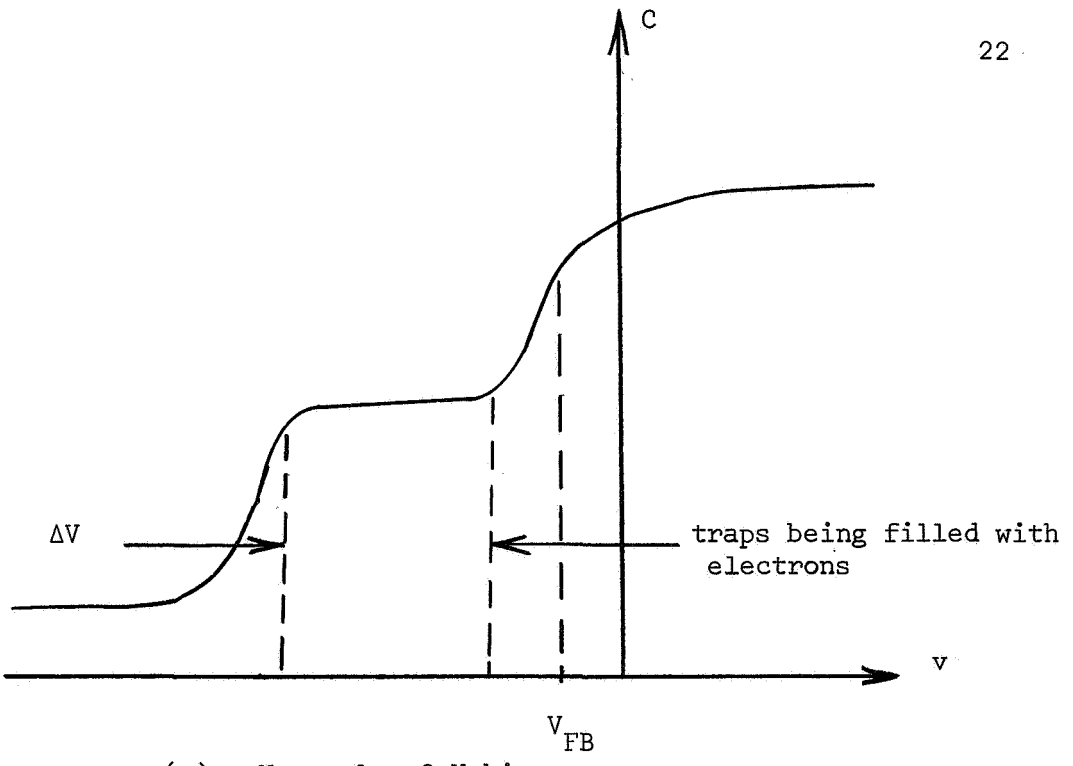
$$\Delta V = \frac{Q_{ss}}{C_I} = \frac{qN_{ss}}{C_I} \quad . \tag{12}$$

The resulting C-V curve is shown in Figure 8a. One observes essentially a plateau in the C-V curve during the interval over which the surface states are becoming filled.

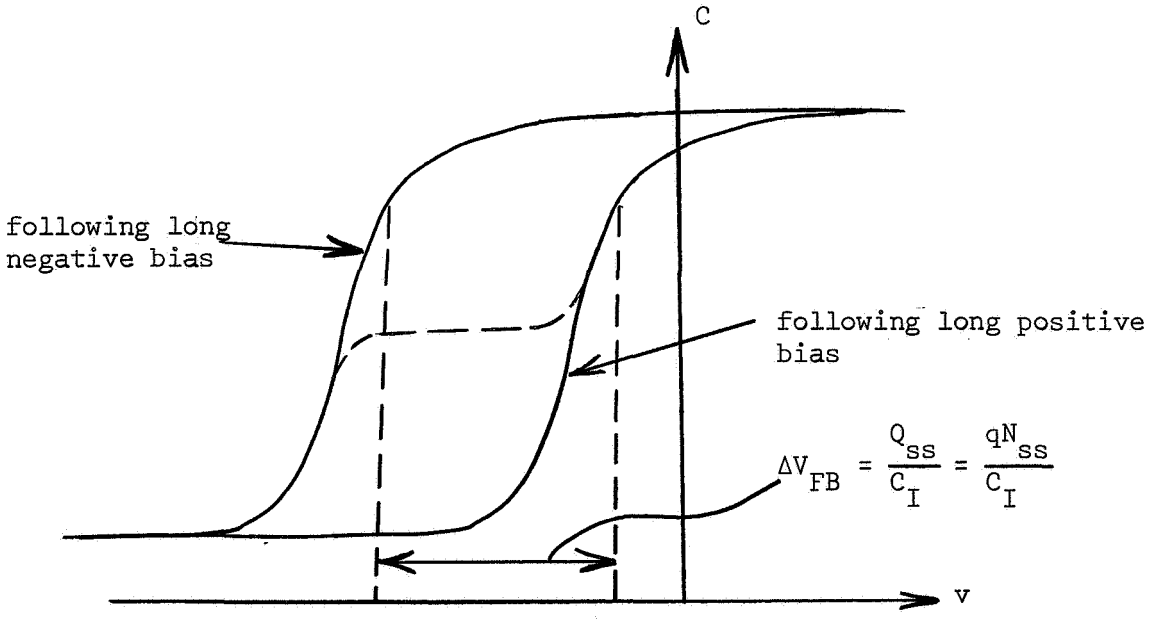
Typical C-V curves for the same case with a fast bias sweep are shown in Figure 8b. In this case one observes an ideal C-V curve displaced along the voltage axis with the displacement or flat-band voltage depending on the history of the device prior to making the fast bias sweep. Typical curves are shown following a long negative bias when the surface states are all empty and following a long positive bias when the surface state are all filled. The difference in flat band voltage between the above two cases is related to the total number of surface states as indicated in the figure.

The case of a discrete surface state level is probably the simplest case of an MIS instability or time dependent effect. Rarely does one encounter a dominant single energy surface state, but rather most devices have surface states which are distributed in energy within the forbidden band. Typical C-V curves for this case are shown in Figure 9. Distributed surface states cause a gradual change in the C-V curve from the ideal C-V curve, because the surface state charge is gradually changing at all bias voltages. Again in this case as shown in Figure 9b, a fast bias sweep can be used to study the charge state of the surface states at any given time.

In addition to instabilities due to bias dependent surface state charge densities, in real insulators there are bias and time dependent bulk insulator charge densities. To discuss these effects consider an MIS device with no surface states and only a bulk insulator charge density.

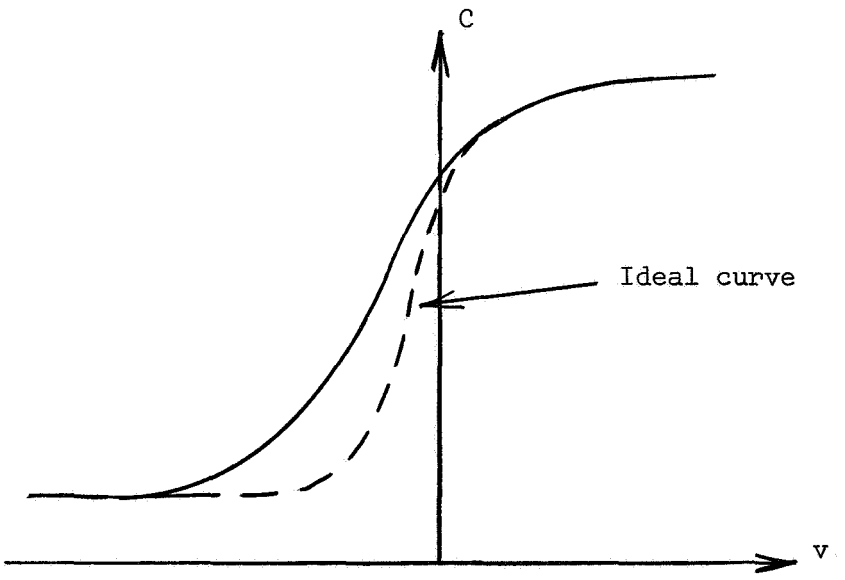


(a). Very slow C-V bias sweep

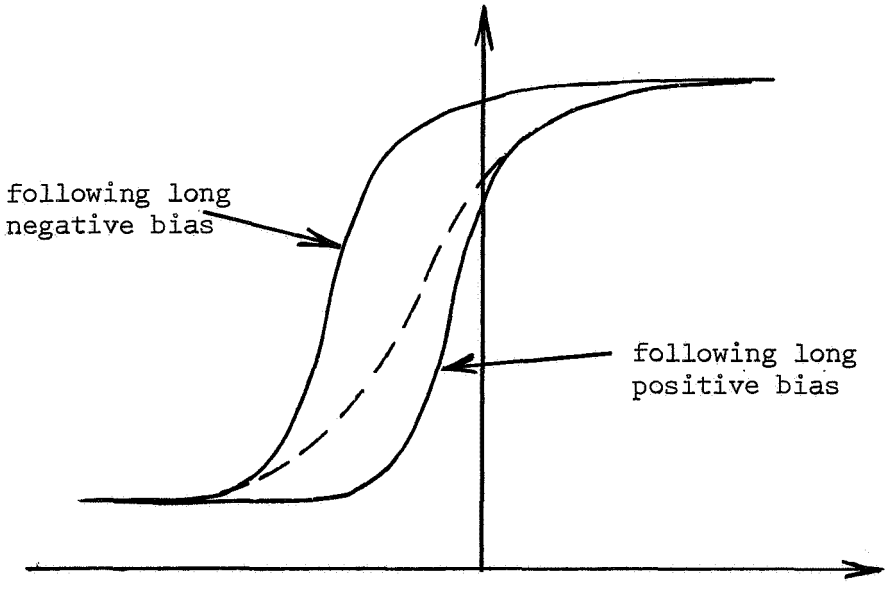


(b). Fast C-V bias sweep

Figure 8. C-V curves for a discrete surface state within the forbidden band.



(a). Very slow C-V bias sweep



(b). Fast C-V bias sweep

Figure 9. C-V curves for distributed surface states

As previously discussed this charge can arise from ions within the insulator or from electrons and holes (electronic charges) within the insulator. The effects of each of these on the C-V curves will be considered separately.

The bias dependent effects of ions on C-V curves is well known from the large amount of work done on SiO_2 where the ionic instability is the dominant instability [1]. With a positive gate bias, positive ions within the insulator tend to drift toward the insulator-semiconductor interface. This causes an increase in the integral

$$\int_o^L \frac{x}{L} \rho(x)dx, \tag{13}$$

and consequently the flat-band voltage as given by Equation (4) shifts to larger negative values for a positive bias. Implicit in this statement is the assumption that the ions remain in the insulator and are not able to cross the insulator-semiconductor boundary or the metal-insulator boundary. Ionic instabilities are normally such slow processes that one rarely observes a slow C-V bias sweep curve, but rather one normally observes a fast bias sweep curve. This simply gives the ideal C-V curve displaced along the voltage axis as shown in Figure 10. Typical curves are shown for ion drift relative to an initial curve following a positive bias and following a negative bias. It is important to note that for the ionic instability a positive bias causes the C-V curve to drift with time in the negative voltage direction, while a negative bias causes a drift of the C-V curve along the voltage axis in the positive voltage direction. This direction of drift is opposite to that of the electronic type of instability to be discussed next.

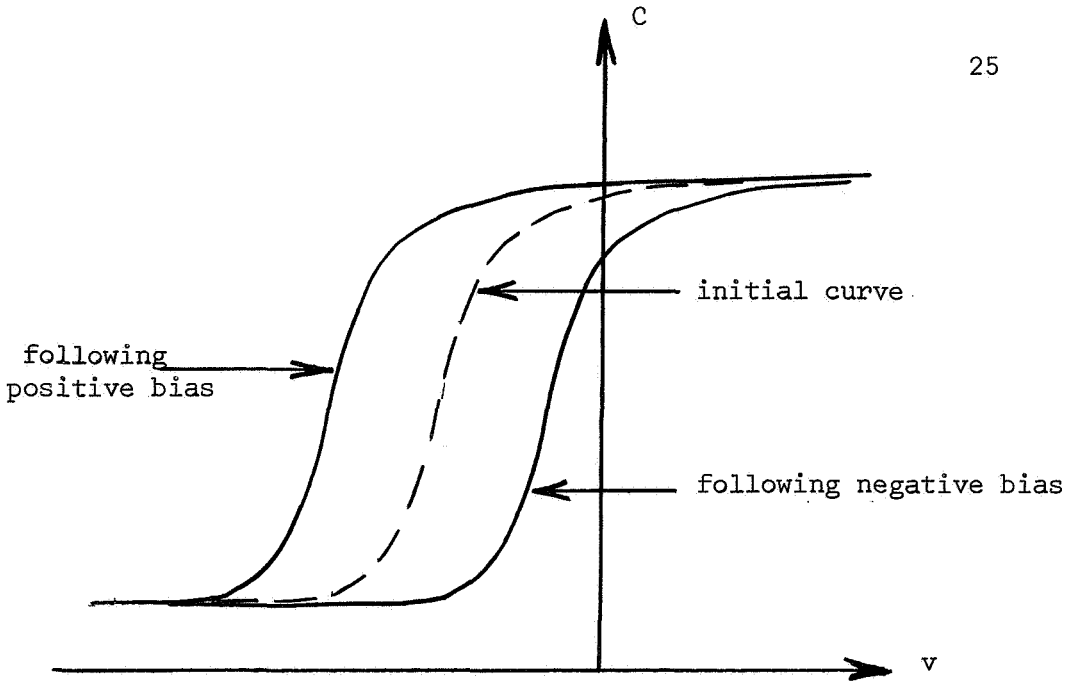


Figure 10. Shifts in C-V curves for ion drift in insulator with fast C-V bias sweep.

Consider next the case of electronic charges (either electrons or holes) within the insulator and the effect of a negative bias on this electronic charge density. Any electrons trapped within the insulator are able, as they are released from traps, to flow toward the insulator-semiconductor interface and to flow out of the insulator into the semiconductor. This process decreases the negative charge within the insulator or in turn increases the net positive charge within the insulator. Similarly trapped holes can flow out of the insulator across the metal-insulator interface. Hole flow out of the insulator has the opposite effect on the net charge within the insulator to that of electron flow. These processes are sketched in Figure 11.

In addition to electronic charge transport out of the insulator, there is also the possibility of charge injection into the insulator and the subsequent trapping of this charge within the insulator. For a negative bias voltage, holes tend to be injected from the semiconductor

into the insulator while electrons tend to be injected from the metal into the insulator. These processes are illustrated in Figure 12. There are two possibilities for the injection mechanism. It may be thermionic emission over the energy barrier between the metal or semiconductor and the insulator, i.e., Schottky barrier emission, or high field tunneling through the energy barrier, i.e., Fowler-Nordhein emission. The process which dominates depends on the barrier height and the temperature. For low barrier heights and/or high temperatures, Schottky emission tends to dominate, while for large barrier heights and low temperatures, Fowler-Nordhein emission tends to dominate [22].

The combined effects of electronic charge injection and charge flow out of the insulator can lead to some rather complex possible shifts in the C-V curves under an applied bias. If the insulator has a large electron

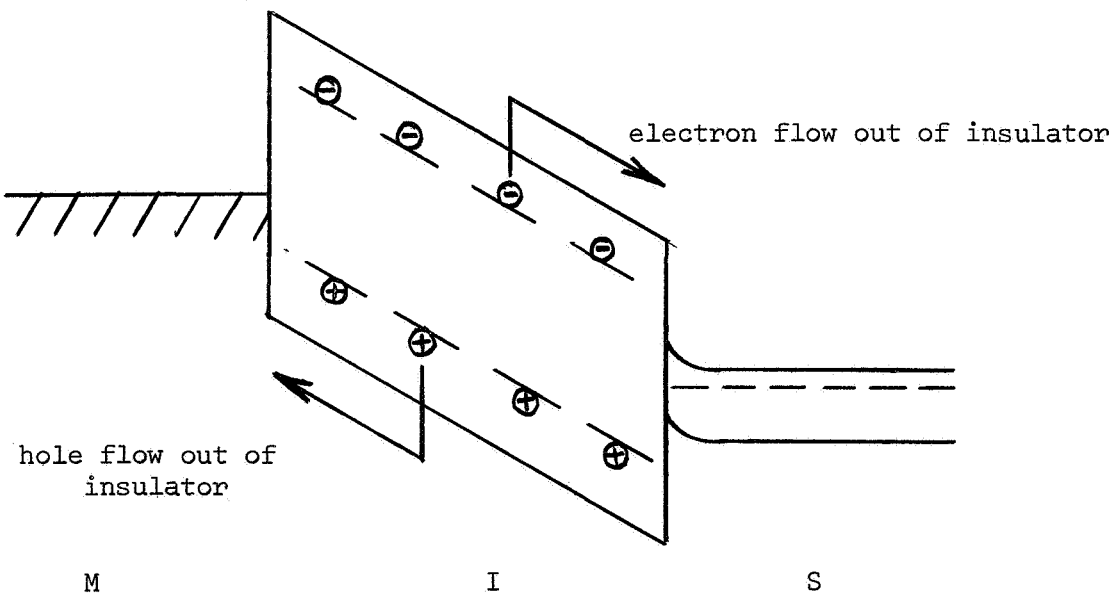


Figure 11. Electronic charge flow out of the insulator for a negative bias

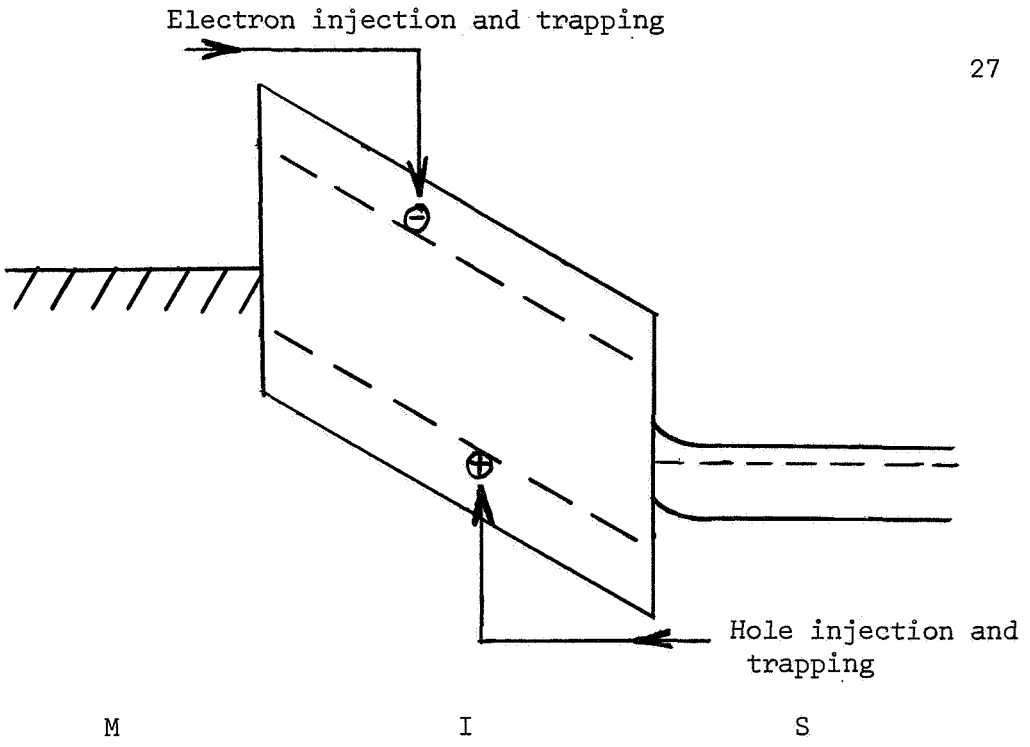


Figure 12. Charge injection into the insulator with subsequent trapping of charges, for negative bias.

and hole trap density, then it is to be expected that most of the charge changes occur near the boundaries of the insulator. For example, under a negative bias and in the region near the semiconductor-insulator interface, electrons can flow from the insulator into the semiconductor and holes can be injected into the insulator becoming trapped near the interface. Both of these processes lead to an increase in the positive charge density in the insulator near the semiconductor. The opposite processes occuring near the metal interface can lead to an increase in the negative charge density near the metal. With a large insulator trap density which is typical of most practical insulators the term

$$\int_0^L \frac{x}{L} \rho(x)\, dx, \tag{14}$$

tends to become more positive under a negative bias corresponding to the increased positive charge near the semiconductor. Thus for this

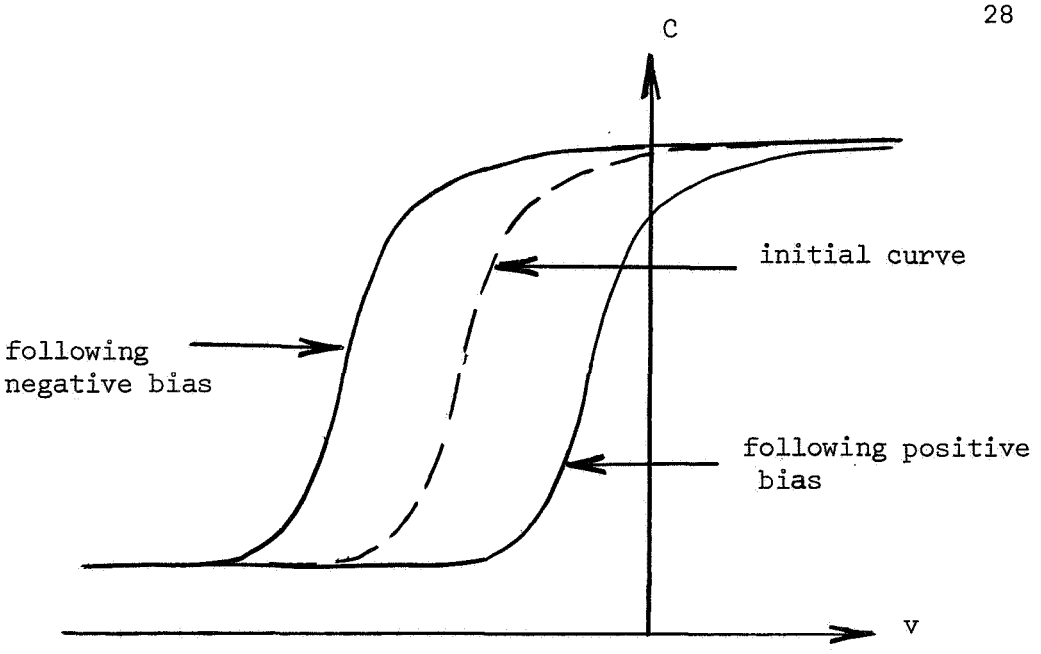


Figure 13. Shifts in C-V curves for electronic injection into insulator with fast C-V bias sweep.

electronic type of instability, the flat-band voltage tends to shift to larger negative voltages under a negative bias, and to shift to larger positive voltages under a positive bias. This is illustrated in Figure 13 for the fast bias sweep case.

Comparing Figures 10 and 13 it is seen that the flat band voltage shift for the electronic type of instability is in the opposite direction to that of the ionic type of instability. This provides a means of distinguishing between these two types of instabilities. For example, if the flat-band voltage becomes more negative for a positive bias one has the ionic instability, while a shift of the flat-band voltage to more positive values indicates an electronic type of instability. The different behavior in the two cases arises from the fact that in the electronic case charges are free to cross the insulator boundary while the ions are confined to the insulator and can only pile-up at the boundaries of the insulator.

A comparison of Figures 9 and 13 show that the charging and discharging of surface states causes the same bias dependent shifts in the fast bias sweep C-V curve as that caused by the bulk electronic type of instability. Thus there can be a question in any given case as to whether an observed instability of this type arises from surface states or from bulk electronic processes within the insulator. In acutal cases there is probably no simple way of distinguishing between these possibilities. The time dependence of the effects can be a help in suggesting which type of instability is being observed. With surface states one expects to reach equilibrium in fairly short times, certainly within times on the order of seconds. Thus if one observes an instability of this type which takes days to reach equilibrium it is likely a bulk electronic type of instability. Of course one can postulate some type of surface state creation process which has as long a time constant as desired. Such speculation provides fertile grounds for those versed in complex model building. Bulk electronic effects appear to be more likely explanations for long time instabilities then such speculations—especially if the observations can be explained on the basis of well established physical principles.

The instabilities normaly observed with SiO_2 insulators are of the ionic type with a relatively small density of fast surface states. Recently on very pure, i.e. free from ions, oxides there has been some evidence of the electronic type of instability at elevated temperatures [7]. With Si_3N_4 insulators, as studied in this work, the instability is decidely of the electronic type, and large shifts in the C-V curve can be observed at room temperature in times of less than one secnnd. The remainder of this work is devoted to a model for the charge injection, electronic instability in insulators and experimental data on this phenomena for silicon nitride MIS devices.

3. SCHOTTKY BARRIER INJECTION MODEL FOR ELECTRONIC TYPE OF INSTABILITY

In the previous chapter a general discussion is presented on the various types of charge instabilities present in MIS devices, and the effects of these charge instabilities on C-V measurements. The ionic and surface state types of instability have previously been investigated in much detail by many investigators. In addition, this work grew out of an experimental study of charge instabilities in silicon nitride insulator layers on silicon substrates, where the electronic instability dominates. Consequently this chapter is devoted to a more thorough investigation of the electronic type of instability. These are bulk processes occuring in the insulator involving the flow of electrons or holes across the insulator-semiconductor boundary.

As discussed in the previous chapter, the electronic type of instability can arise from the release of trapped carriers within the insulator and the flow of these carriers out of the insulator or from the injection of carriers into the insulator and the subsequent trapping of the carriers within the insulator. The present work is concerned only with the injection and trapping of carriers. A previous report has discussed in some detail the release of carriers from traps and the flow out of the insulator [12]. Carriers must be trapped fairly deeply in the insulator in order to neglect any release of these from traps. For carriers which are trapped at energies deeper than 1.0 ev, one can estimate the release time as 10^4 sec or longer using an attempt to escape frequency of 10^{11}/sec. This time of 10^4 sec represents about the longest time intervals considered in this work. Thus to neglect carrier release we must assume that the carriers are trapped at energies deeper than 1.0 ev from the conduction bands.

The energy band diagram between a metal and a wide band-gap semiconductor or insulator is shown in Figure 14. The image force for an electron or hole in the insulator and semiconductor is shown by the dotted barrier in the figure. In equilibrium an electron must overcome an energy barrier ϕ_o to go from the metal into the insulator. With an applied field as shown in Figure 14(b) the barrier between the metal and insulator is lowered by an amount $\Delta\phi$ because of the image force. This is the familiar Schottky barrier lowering effect, and it is known that [24]

$$\Delta\phi = \frac{1}{2}\sqrt{\frac{qE_s}{\pi\varepsilon}} \quad , \tag{15}$$

where E_s is the electric field in the region near the interface. Electrons from the metal crossing the barrier constitute a current which has been shown to be of the form

$$J_s = A \exp\left(B\sqrt{E_s}\right) , \tag{16}$$

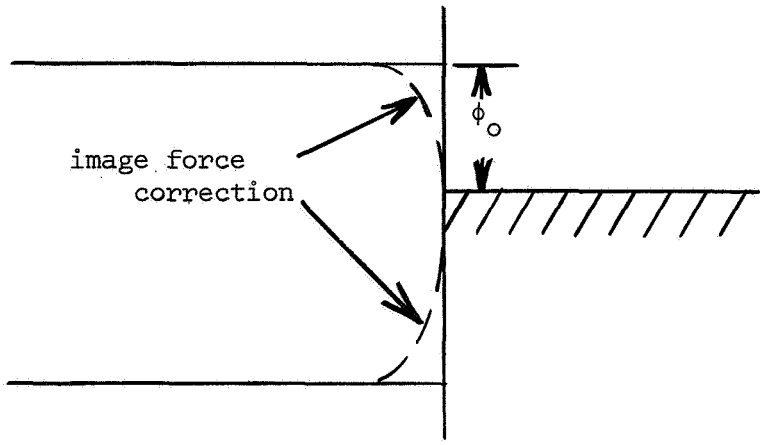
where

$$A = \frac{4\pi q m k^2 T^2}{h^3} \exp\left(-qV_o/kT\right) \tag{17}$$

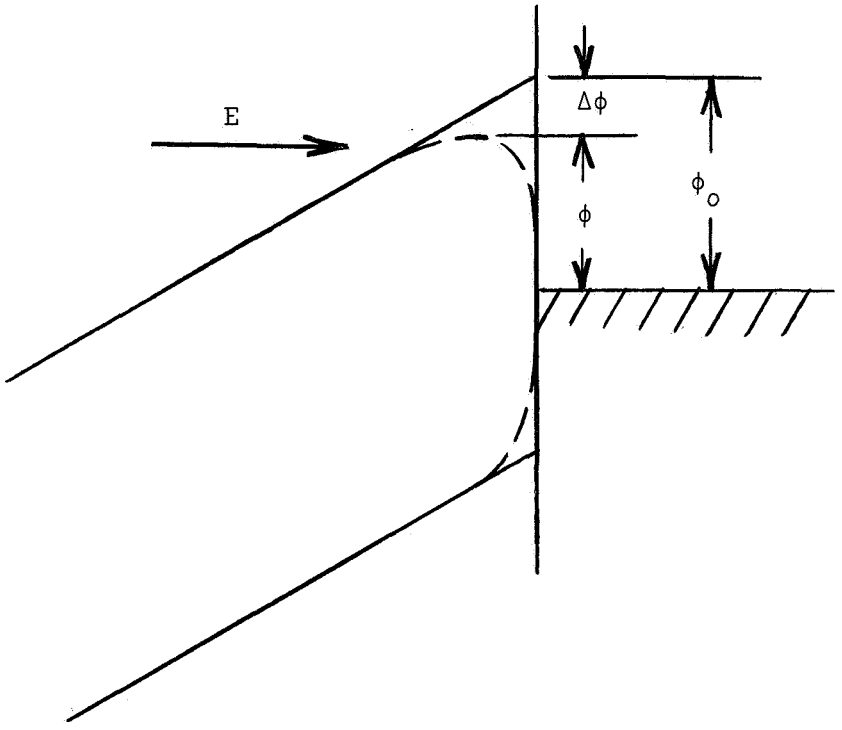
$$B = \frac{q}{2kT}\sqrt{\frac{q}{\pi\varepsilon}} \tag{18}$$

and V_o is the initial barrier potential ($qV_o = \phi_o$). The current density increases as the electric field is increased because of the increased barrier lowering with increased field.

The Schottky current is a flow of thermal carriers over a potential barrier as shown in Figure 14. An additional component of current can arise from carriers which tunnel through the barrier. This is the so-called Fowler-Nordheim current which is of the form [24]



(a) Zero applied field



(b) Large applied electric field

Figure 14. Energy band diagram between a metal and an insulator

$$J_s' = DE_s^2 \exp(-C/E_s) , \tag{19}$$

where

$$C = \frac{4}{3}\left(\frac{2m}{\hbar^2}\right)^{1/2} V_o^{3/2} , \tag{20}$$

$$D = \frac{q}{2\pi h(V_o+V_F)} \sqrt{\frac{V_F}{V_o}} , \tag{21}$$

and $V_F = q\phi_F$ is the potential corresponding to the Fermi energy in the metal. The Fowler-Nordheim current also increases with increasing field because of the increased tunneling probability through the reduced barrier width.

In any practical case both Schottky current and Fowler-Nordheim current will be present. Because of the exponential dependence of the Schottky current on the barrier height V_o, it becomes extremely small for large barrier heights. For low barrier heights and/or high temperatures, Schottky current is known to dominate. The present work considers in detail only the Schottky current as this appears to be the dominant current for silicon nitride films.

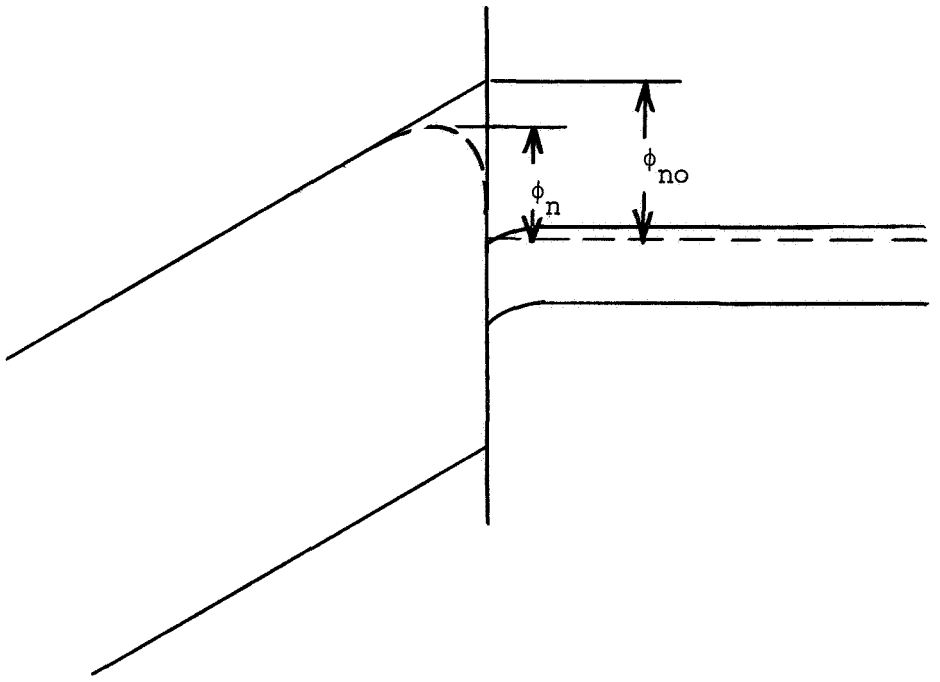
The above discussion and figures have considered a metal-insulator barrier. In MIS devices the barrier of major interest is that between the insulator and the semiconductor. Since the Schottky current involves only those carriers far above the Fermi level, it makes little difference whether one is considering injection from a semiconductor or from a metal as long as one remembers that the barrier of importance is that between the conduction band of the insulator and the Fermi level at the surface of the semiconductor. However, the Fermi level at the surface of the semiconductor is a function of the electric field at the surface. Thus one has an additional means by which the Schottky barrier can change in addition to the normal image force effect. The Fermi level variation at the surface of the semiconductor is limited to roughly the width of

the semiconductor band gap. In strong accumulation the surface Fermi level is above but close to the conduction band edge, while in strong inversion the surface Fermi level is below but close to the valence band edge. This is illustrated in Figure 15 for an n-type semiconductor. For strong accumulation, the injection barrier is ϕ_n for electrons, and for strong inversion one has an injection barrier ϕ_p for holes. If one can determine the electron injection barrier ϕ_n (and ϕ_{no}) under strong accumulation, and the hole injection barrier ϕ_p (and ϕ_{po}) under strong inversion it is possible to obtain the insulator band gap E_{gi} from the approximate expressions

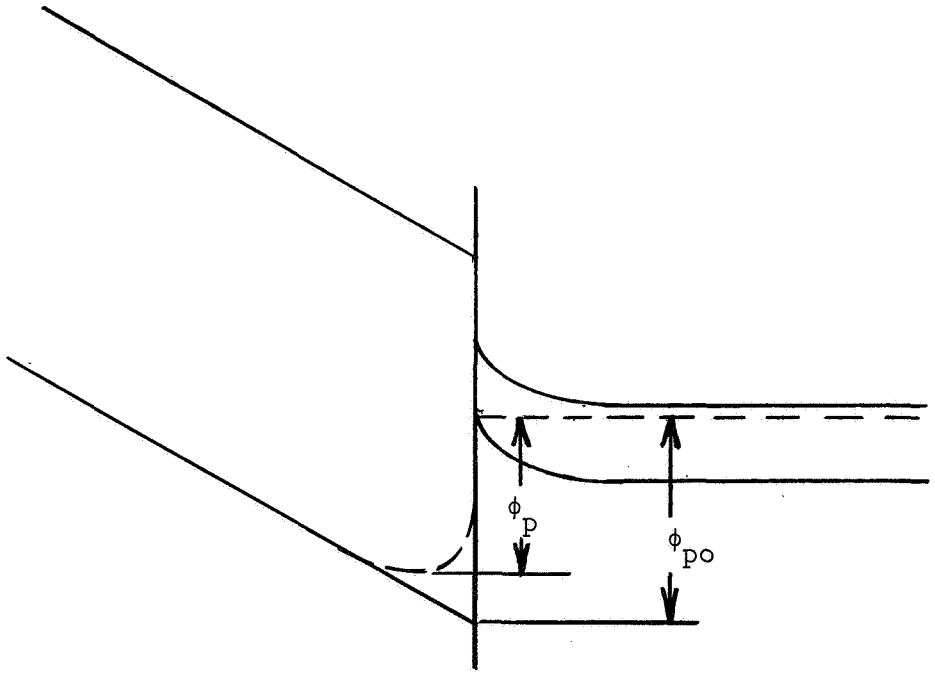
$$E_{gi} \simeq \phi_{no} + \phi_{po} + E_{gs}, \tag{22}$$

where E_{gs} is the semiconductor band gap. In this work it will be assumed that the bias voltages on an MIS structure are always such as to have either the strong accumulation condition or the strong inversion condition. Thus the electron barrier ϕ_{no} is taken as the difference between the conduction band energies in the insulator and semiconductor, and the hole barrier ϕ_{po} is taken as the difference between the valence band energies in the insulator and the semiconductor. Any small penetration of the Fermi level above the conduction band or below the valence band is neglected in this work.

A voltage applied across an MIS device establishes an electric field at the insulator-semiconductor interface, and this in turn gives rise to a Schottky barrier injected current as given by Equation 16. Consider the case of a large positive bias as shown in Figure 15(a). The electrons injected over the Schottky barrier into the insulator constitute an excess of carriers above the equilibrium value. These carriers may either continue



(a) Strong accumulation (positive metal bias)



(b) Strong inversion (negative metal bias)

Figure 15. Energy barriers for strong accumulation and strong inversion.

in the conduction band and flow out of the insulator at the metal boundary, or they may become trapped in the insulator. This trapping process has been illustrated in Figure 12. Whether a carrier becomes trapped or continues through the sample depends on the ratio of carrier transit time τ_{tr} to trapping time τ_{tp}. The transit time is given by the expression

$$\tau_{tr} = \frac{W_I}{\mu \bar{E}} \quad , \tag{23}$$

where $\bar{E}$ is the average electric field in the insulator. For typical parameters ($W_I = 10^{-5}$cm, $\mu = 10\text{cm}^2/\text{v.sec.}$, $E = 10^6$v/cm) $\tau_{tr} = 10^{-13}$ sec. This probably represents a lower limit on the transit time because the mobility may be considerably less than $10\text{cm}^2/\text{v.sec.}$ If the trapping time is less than the transit time, most of the carriers become trapped in the insulator. On the other hand if the transit time is less than the trapping time only the fraction τ_{tr}/τ_{tp} of the carriers become trapped in the insulator.

Regardless of the ratio of transit-to-trapping time at least some of the carriers become trapped in the insulator, and this Schottky barrier injection mechanism represents an instability because of the bias and time dependent trapped charge within the insulator. To illustrate the type of electronic instability which this injection gives rise to, consider the case of an MIS device which initially has no charge within the insulator and which at t = o is subject to a large positive bias V applied to the metal electrode. Neglecting the small potential drop within the semiconductor, the initial electric field within the insulator is uniform and of the magnitude.

$$E_s(t=o) \simeq \frac{V}{W_I} \quad . \tag{24}$$

This gives rise to an initial Schottky barrier electron current density of

$$J_{ns}(t=o) = A \exp\left(B \sqrt{\frac{V}{W_I}}\right). \tag{25}$$

Part of these carriers become trapped within the insulator on trap sites. As soon as charge begins to build up within the insulator, some of the field lines from the metal electrode terminate on these and the field at the interface begins to decrease, i.e.

$$E_s\ (t>o) < E_s\ (t=o)\ . \tag{26}$$

With the field at the interface becoming reduced, the injected Schottky current as given by Equation 16 decreases, and the process continues but at a slower rate. Thus the process gives a continuous build-up of trapped electrons within the insulator with a continuous reduction in the Schottky barrier current crossing the barrier. The remainder of this chapter is devoted to developing a model for the time dependence of this Schottky barrier injection instability following the application of a voltage pulse to an MIS device.

At any instant of time the current density crossing the Schottky barrier current is given by the equation

$$J_{ns}(t) = A \exp\left[B \sqrt{E_s(t)}\right], \tag{27}$$

where $E_s(t)$ is the time dependent field at the barrier interface. The electric field is related to the applied voltage and the charge within the insulator by the expression

$$E_s(t) = \frac{V}{L} + \int_o^L \frac{x}{L} \frac{\rho(x,t)}{\varepsilon}\ dx, \tag{28}$$

where $\rho(x,t)$ is the trapped charge density as a function of position and time. The integral can only be evaluated exactly if the spatial dependence of trapped charge is known. However, two interesting limiting cases can be considered.

Consider first the case where the trapping time is very short compared with the transit time. In this case all the injected charge is trapped near the interface i.e. near X = L and the above equation becomes

$$E_s(t) = \frac{V}{L} + \frac{\sigma(t)}{\varepsilon} \quad , \tag{29}$$

where $\sigma(t)$ is the total charge per unit area within the insulator. The other case which can be easily solved is that in which the charge is trapped uniformly within the insulator. This would be the case when the transit time is very short compared with the trapping time. In this case

$$E_s(t) = \frac{V}{L} + \frac{1}{2}\frac{\sigma(t)}{\varepsilon} \quad , \tag{30}$$

which shows that the total charge is only half as effective in reducing the surface electric field. Any actual case will be somewhere between these extreme cases and we can write

$$E_s(t) = \frac{V}{L} + \delta\frac{\sigma(t)}{\varepsilon} \quad , \tag{31}$$

as long as the trapped charge distribution monotonically decreases from the semiconductor toward the metal boundary, δ will be in the range from 0.5 to 1.0 .

The two extreme cases considered above correspond to very small and very large ratios of the trapping-to-transit time. By considering these two limiting cases, it is possible to obtain an indication of the time behavior of Schottky barrier injection under all conditions. Consider first the short trapping-to-transit time case. All of the Schottky

current goes into traps, so we can write

$$\frac{d\sigma(t)}{dt} = - J_s(t) = - A \exp (B \sqrt{E_s} \quad . \tag{32}$$

The negative sign arises because of the negative electron charge. When this is combined with Equation (29), a single differential equation for $\sigma(t)$ is obtained, which is

$$\frac{d\sigma}{dt} = - A \exp \left[B \sqrt{\frac{V}{L}} \sqrt{1 + \frac{L\sigma}{V\varepsilon}} \right]. \tag{33}$$

It should be recalled that σ is a charge density per unit area of electrons and is negative. The quantity $1 + \frac{L\sigma}{V\varepsilon}$ thus decreases as time proceeds and as the carriers become trapped.

Before considering the exact solution to Equation (33), it is useful to consider an approximate solution for small densities of trapped charge. If at $t = o$ we have the case $\sigma \approx o$, then for some finite time interval we will have $L\sigma/V\varepsilon << 1$. During this time interval we have

$$\frac{d\sigma}{dt} \simeq - A \exp \left[B \sqrt{\frac{V}{L}} \left(1 + \frac{L\sigma}{2V\varepsilon} \right) \right]. \tag{34}$$

The solution of this is

$$\sigma = - \frac{2\varepsilon}{B} \sqrt{\frac{V}{L}} \ln (1 + t/\tau_o) \ , \tag{35}$$

where

$$\tau_o^{-1} = AB \sqrt{\frac{L}{V}} \quad \frac{1}{2\varepsilon} \quad \exp (B \sqrt{\frac{V}{L}} \ ) \ . \tag{36}$$

This predicts essentially two regions of different time dependence, which are:

$$\begin{aligned} &\sigma \propto t \quad \text{for} \quad t << \tau_o \\ &\sigma \propto \ln t \quad \text{for} \quad t >> \tau_o \ . \end{aligned} \tag{37}$$

For large values of time, or correspondingly for large values of injected charge density σ, the expansion leading from Equation (33) to Equation (34) is no longer valid, and the simple solution is not valid.

An exact solution of Equation (33) results in the transcendental equation

$$\frac{Z + 1}{Z_o + 1} \exp (Z_o - Z) = 1 + t/\tau_o , \tag{38}$$

where

$$Z = B \sqrt{\frac{V}{L}} \sqrt{1 + \frac{L\sigma}{V\epsilon}} , \tag{39}$$

$$Z_o = B \sqrt{\frac{V}{L}} . \tag{40}$$

The parameter Z_o is simply the initial Schottky barrier lowering at $t = 0$ divided by kT, while Z is the Schottky barrier lowering at any later time t divided by the same factor kT, i.e. $Z = \Delta\phi/kT$. With an initial field of 10^6 v/cm and a dielectric constant of 4 (Si_3N_4), the initial barrier lowering is approximately 0.19 ev, so $Z_o \simeq 7.3$. Values of Z_o in the range of 10 or slightly larger can be achieved with reasonable voltage in MIS devices. It should also be noted that the dielectric constant involved in the equations is that of the insulator very near the insulator-silicon interface and this may be different from the bulk dielectric constant.

The general solution of Equation (38) reduces to that of Equation (34) for $Z_o >> 1$ and for $Z_o - Z << Z_o$. The change in normalized barrier lowering $\Delta Z = Z_o - Z$ as a function of time is shown in Figure 16 for varying amounts of initial barrier lowering. The limiting curve $Z_o \to \infty$ is the same as that corresponding to Equation 34. The curves are shown terminating at the point

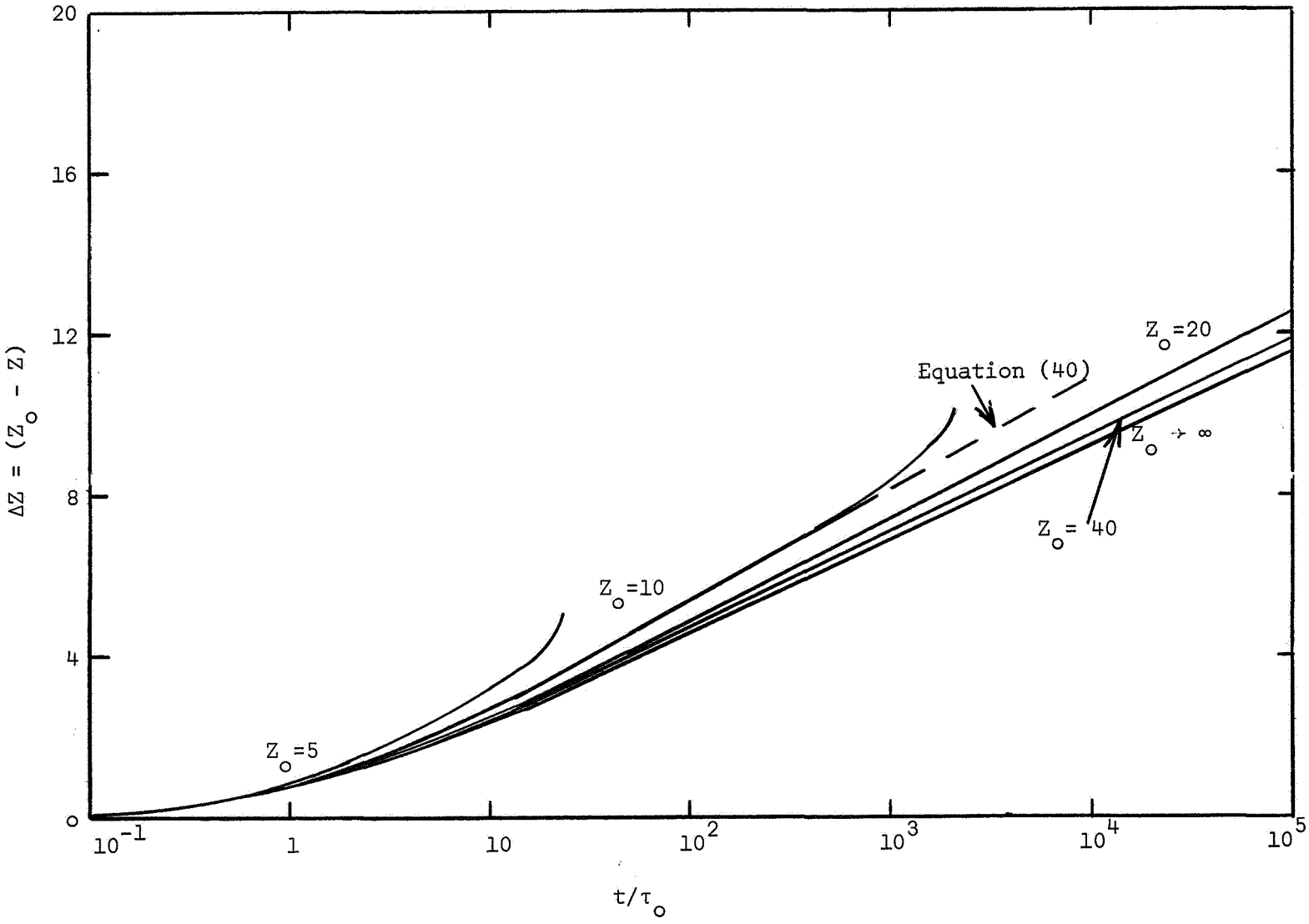


Figure 16. Change in barrier height as a function of time ($Z = \Delta\phi/kT$)

$\Delta Z = Z_o$ since at this point the barrier lowering equals zero. At this point enough charge has been injected into the insulator and trapped in the insulator to reduce the field to zero at the interface. This is the limiting amount of charge which can be injected into the insulator. A fairly good approximation to the curves in Figure 16 is given by the equation

$$\Delta Z \simeq \left(\frac{Z_o + 2}{Z_o}\right) \ln (1 + t/\tau_o). \tag{41}$$

In the limit of large Z_o this becomes the exact solution. Points given by this approximation are also shown in the figure for $Z_o = 10$.

The time dependence of injected and trapped charge in the insulator is shown in Figure 17. The particular normalization constant for the charge, i.e. the combination $L\sigma Z_o/\varepsilon V$, has been chosen so that the solution for the entire range of Z_o values can be conveniently shown on a single graph. For large values of Z_o it is seen that the injected charge density σ varies approximately linearly with $\ln(t)$ over a large range of time. The interesting injection phenomena is seen to cover a large range of times. For example with $Z_o = 20$ significant charge injection effects occur over more than five orders of magnitude in time.

This dependence of injected charge on ln(t) presents some difficulties in experimentally observing Schottky barrier injection. For example if $\tau_o = 1$ sec and Z_o is large, one observes essentially the same amount of injected charge between 10 sec and 10^2 sec as is observed between 10^2 sec and 10^3 sec and subsequently is observed between 10^3 sec and 10^4 sec. Thus to observe the total effect one must be able to observe short time changes in injected charge as well as wait very long times to reach a steady state condition.

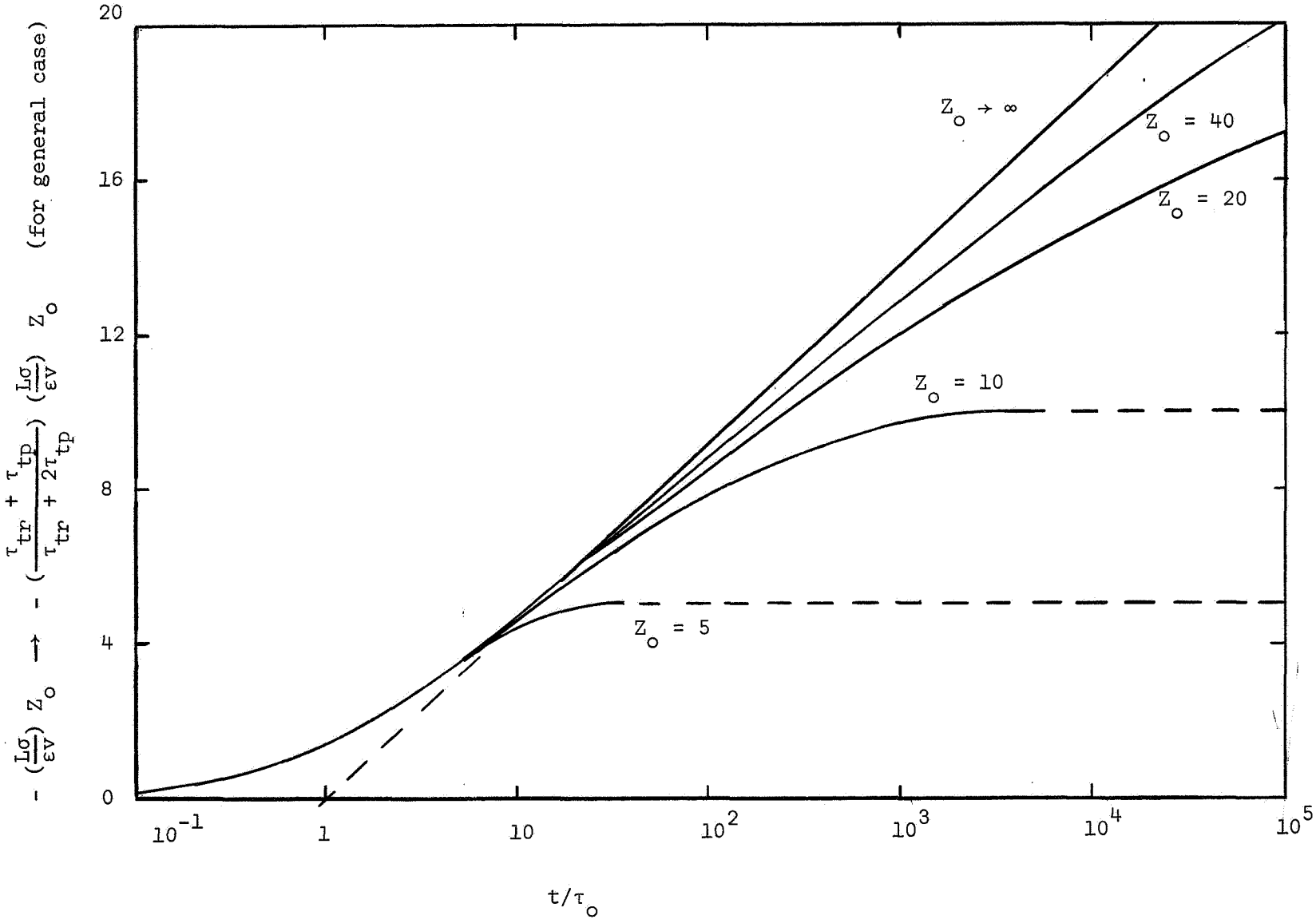


Figure 17. Change in trapped charge as a function of time

The above discussion has been for the case where the trapping time is short compared with the transit time, and the charge is trapped very close to the semiconductor interface. Now consider the opposite case where the transit time is very short compared with the trapping time, and trapping occurs uniformly throughout the insulator. Only the fraction τ_{tr}/τ_{tp} of injected charges become trapped within the insulator so

$$\frac{d\sigma}{dt} = - \frac{\tau_{tr}}{\tau_{tp}} J_s(t). \tag{42}$$

Combining this with Equations (27) and (30) gives

$$\frac{d\sigma}{dt} = \frac{\tau_{tr}}{\tau_{tp}} A \exp \left[B \sqrt{\frac{V}{L}} \sqrt{1 + \frac{L\sigma}{2V\varepsilon}} \right] . \tag{43}$$

Comparing this equation with Equation (33) for the fast trapping case, it is seen that the only difference is that A is replaced by A $\tau_{tr}/2\tau_{tp}$ and σ is replaced by $\sigma/2$. Since the transit time is field dependent, there is some dependence of the factor τ_{tr}/τ_{tp} on the trapped charge σ. However if one keeps a constant bias voltage on an MIS device, the average electric field within the insulator must remain constant. Consequently the average electron velocity is independent of σ. This means that the change in τ_{tr}/τ_{tp} with σ is smaller than might at first be expected. For this reason this ratio is taken as a constant in our present simple model. Then the solution to Equation (43) is

$$\frac{Z + 1}{Z_o + 1} \exp (Z_o - Z) = 1 + t/\tau_o \tag{44}$$

where

$$Z = B \sqrt{\frac{V}{L}} \sqrt{1 + \frac{L\sigma}{2V\varepsilon}} , \tag{45}$$

$$\tau_o^{-1} = \frac{\tau_{tr}}{2\tau_{tp}} AB \sqrt{\frac{L}{V}} \frac{1}{2\varepsilon} \exp \left(B \sqrt{\frac{V}{L}}\right).$$

A comparison of this solution with Equations(36) and (39) illustrates the similarities between the two cases. They both have the same time dependence. The only difference which appears is a factor of 2 in σ between the equations and a different definition of τ_o^{-1}. The previous solutions shown in Figures 16 and 17 then also apply to the case of short transit-to-trapping time if one simply uses the τ_o defined in Equation (45) and replaces σ by $\sigma/2$.

Since both extreme cases have the same time dependence, it is relatively easy to construct a single solution which reduces to the two limiting cases. Such a solution is given by Equation (44) with

$$Z \simeq B \sqrt{\frac{V}{L}} \sqrt{1+\left(\frac{\tau_{tr} + \tau_{tp}}{\tau_{tr} + 2\tau_{tp}}\right) \frac{L\sigma}{V\varepsilon}} \quad , \tag{46}$$

and

$$\tau_o^{-1} = \left(\frac{\tau_{tr}}{\tau_{tr} + 2\tau_{tp}}\right) AB \sqrt{\frac{L}{V}} \frac{1}{2\varepsilon} \exp\left(B\sqrt{\frac{V}{L}}\right). \tag{47}$$

This solution is expected to be a good approximation to the true solution for all values of τ_{tr}/τ_{tp}. To use Figure 17 for this general case simply requires replacing σ by $[(\tau_{tr} + \tau_{tp})/(\tau_{tr} + 2\tau_{tp})]\,\sigma$ as indicated in the figure. This is not a large correction factor since it only varies between 1 and 2. The biggest change comes in the defining equation for τ_o which is considerably increased for small values of τ_{tr}/τ_{tp}. It is interesting that essentially the same form of time dependence of injected charge is observed for both the case where all the charge is trapped within the insulator and the case where most of the injected charge flows through the insulator and only a small fraction is trapped within the insulator. The important difference is in the time scale where much longer observation times are required for the same change in trapped insulator charge when only a small fraction of the charge is trapped within the insulator.

The Schottky barrier injected charge will be experimentally observable as a shift in flat-band voltage with time. Under the present proposed model this shift will continue until the flat-band voltage has shifted by an amount equal to the applied bias voltage. The theoretical shift in flat-band voltage divided by the applied voltage is shown in Figure 18 for various values of Z_o. The flat-band voltage shift observed by a fast C-V bias sweep then provides a means of studying Schottky barrier injection and trapping phenomena. In this case it is apparent that if the C-V bias sweep occurs in a time which is short compared with τ_o, there will be very little injected charge occuring during the bias sweep.

There are several limitations on the above model which should be recognized in applying the results to practical cases of Schottky barrier injection. First the model has neglected any initial equilibrium charge within the insulator. This will modify the model slightly because the initial electric field at the interface will not be zero as assumed in the normal Schottky model. While this may modify the details of the model somewhat, it is not likely to modify the major features of the model, expecially if the initial equilibrium flat-band voltage is small (on the order of one or two volts).

An additional limitation on the model is the assumption that trapped carriers within the insulator remain trapped for an infinite time. This is obviously unrealistic for very long times even if the carriers are deeply trapped. This causes the injected charge in the proposed model to become large enough to reduce the field to zero at the interface at large values of time. In the actual case, for long values of time some of the trapped carriers will become released from the traps with the release time determining when this occurs. For times longer than the release time for carriers from traps, the presence of significant numbers of released

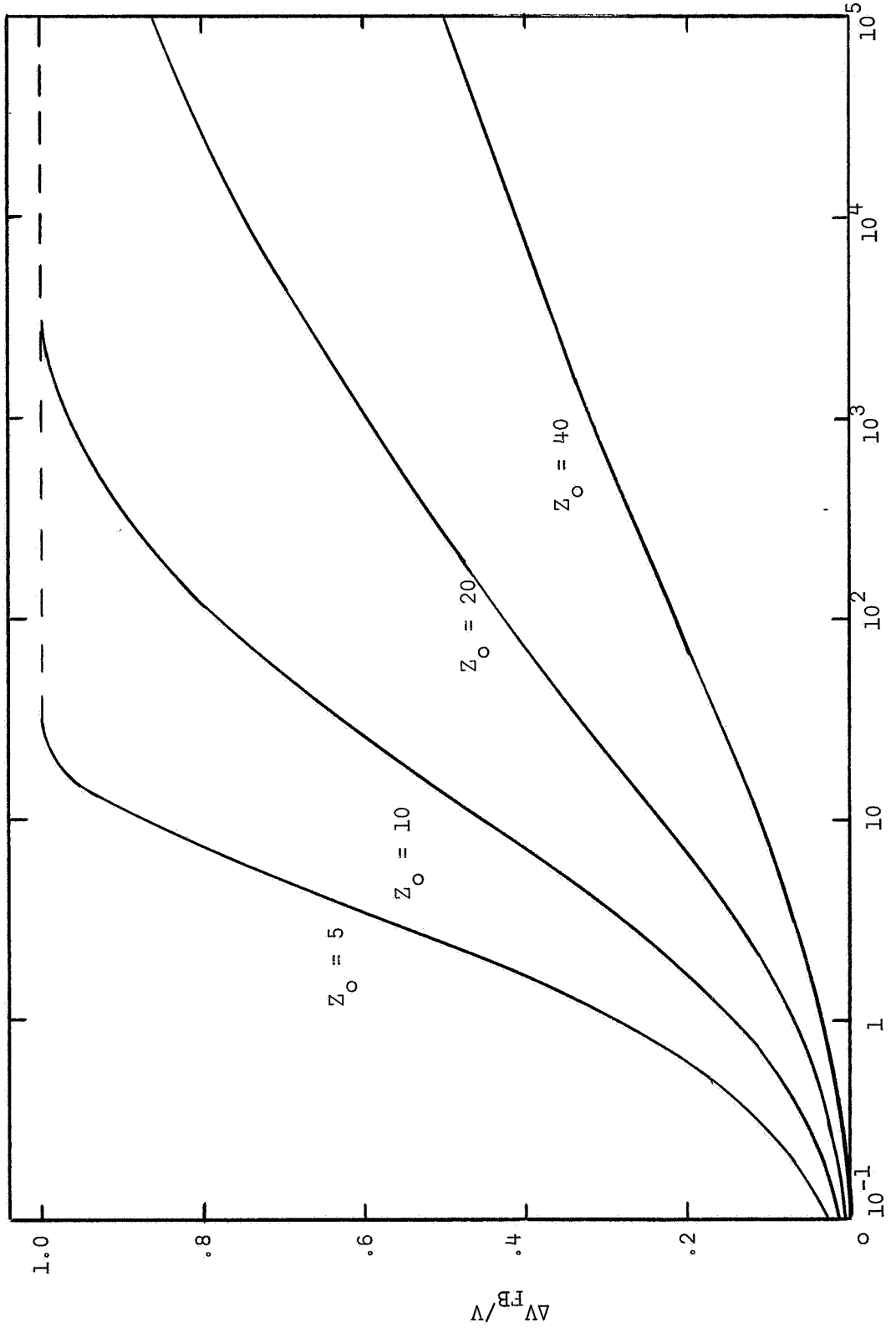


Figure 18. Shift in flat-band voltage with time

carriers will affect the charge build-up process. Some of the released carriers will eventually flow out of the insulator. A steady state condition will be reached when the carriers flowing over the Schottky barrier are just sufficient to replace the carriers which are continually being released from the traps and which are able to flow out of the insulator without becoming retrapped. This requires a non-zero Schottky barrier field to supply this current. The injected charge must then saturate at some value less than that required to reduce the interface field completely to zero. This saturation value of injected charge will depend on the detailed properties of the traps and importantly on the depth of the trap. This release of trapped carriers will have little effect on the initial charge injection model, unless the release time is less than τ_o, and will only become important for times larger than the release time. A sketch of this premature saturation of the injected charge because of trapped carrier release is shown in Figure 19.

The discussion in this chapter has been in terms of an electron Schottky barrier current. The equations and results also apply to hole injection if one has a negative bias voltage. The only change in the equations is the replacement of σ by $-\sigma$ and the use of the appropriate hole injection barrier height.

An interesting feature of the Schottky barrier injection model developed in this chapter is the somewhat surprising independence of the model from the detailed properties of the traps. The time dependence of injected charge is independent of whether the traps are discrete in energy or distributed in energy within the band gap, except at very long times where release time of the traps becomes important.

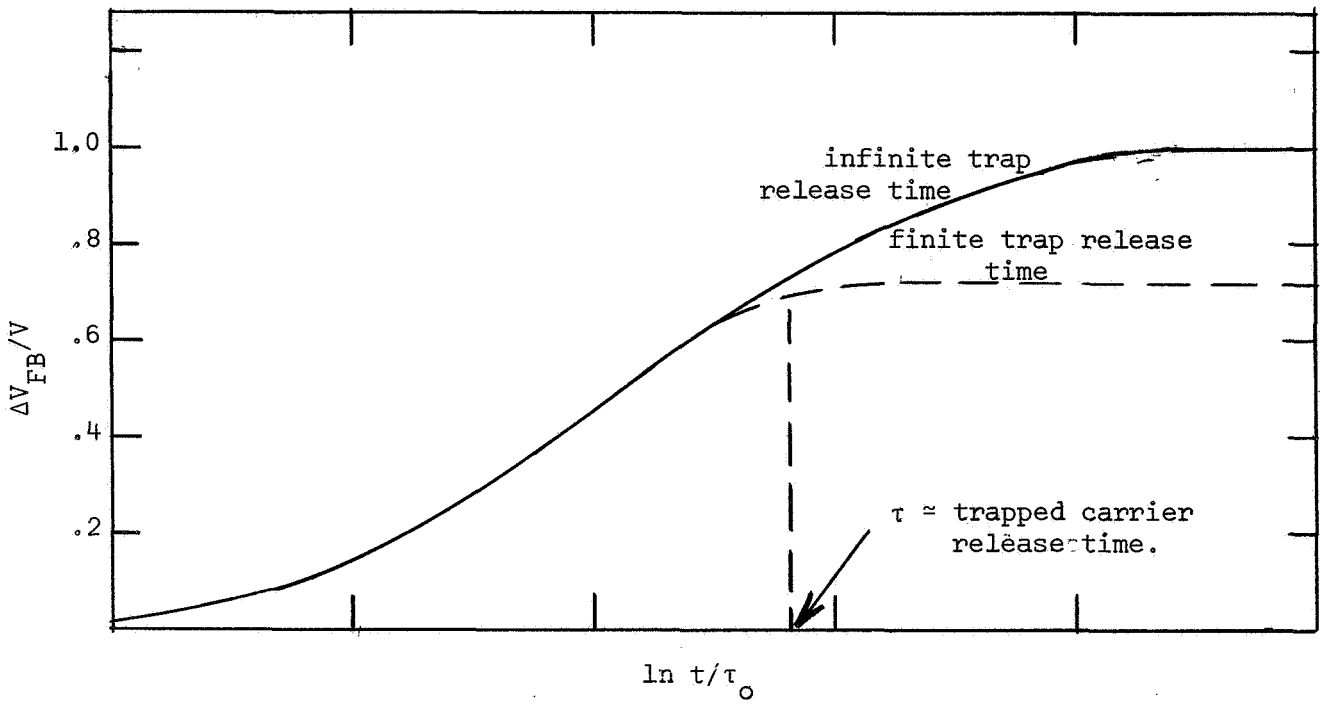


Figure 19. Premature saturation of injected charge because of a finite trap release time.

It is also important to note that the Schottky barrier injection is an intrinsic property of MIS devices as opposed to ion instabilities which can be eliminated by careful manufacturing techniques. Only if one can produce a trap free insulator can one completely eliminate Schottky barrier injection, and this is not likely to occur in the near future. Thus, this type of electronic instability represents a real limitation on MIS devices.

It is useful at this point to consider the magnitudes of the effects due to Schottky barrier injection. The Schottky barrier lowering $\Delta\phi$ is

$$\Delta\phi = (0.379\text{ev}) \left(\frac{\varepsilon_o}{\varepsilon}\right)^{1/2} \left(\frac{V/L}{10^6 \text{v/cm}}\right)^{1/2}, \quad (48)$$

and at room temperature

$$Z_o = 14.6 \left(\frac{\varepsilon_o}{\varepsilon}\right)^{1/2} \left(\frac{V/L}{10^6 \text{v/cm}}\right)^{1/2} \quad (49)$$

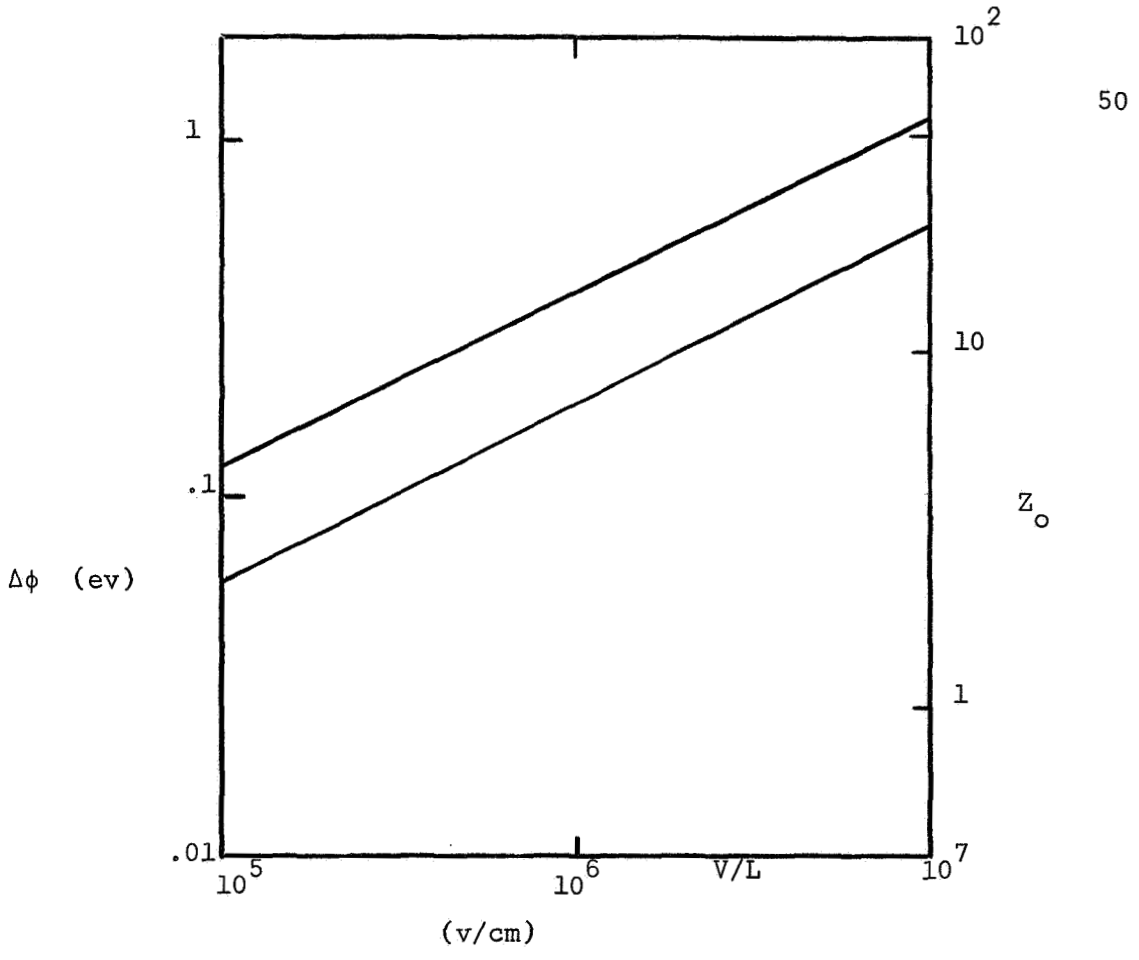


Figure 20. Reduction in barrier height and Z_o at room temperature as a function of applied field

The dependence of $\Delta\phi$ and Z_o on electric field is shown in Figure 20.

The time constant τ_o is given at room temperature by the expression

$$\tau_o = (1.12 \times 10^{-15}\text{sec}) \left(\frac{\varepsilon}{\varepsilon_o}\right)^{3/2} \left(\frac{V/L}{10^6 \text{v/cm}}\right)^{1/2} \times \exp\left(\frac{qV_o}{kT} - Z_o\right). \qquad (50)$$

A sketch of τ_o as a function of barrier height V_o is given in Figure 21 for a field of 10^6v/cm and values of $\varepsilon/\varepsilon_o$ of 1 and 4. The range of times given between 10^{-3} sec and 10^5 sec represents the practical range which one can experimentally investigate. Thus if one is to experimentally observe τ_o at room temperature, the barrier height must be in the range from about 1 ev to about 1.5 ev. It is also noted that τ_o varies quite rapidly with barrier height ϕ_o as well as with the relative dielectric constant of the insulator.

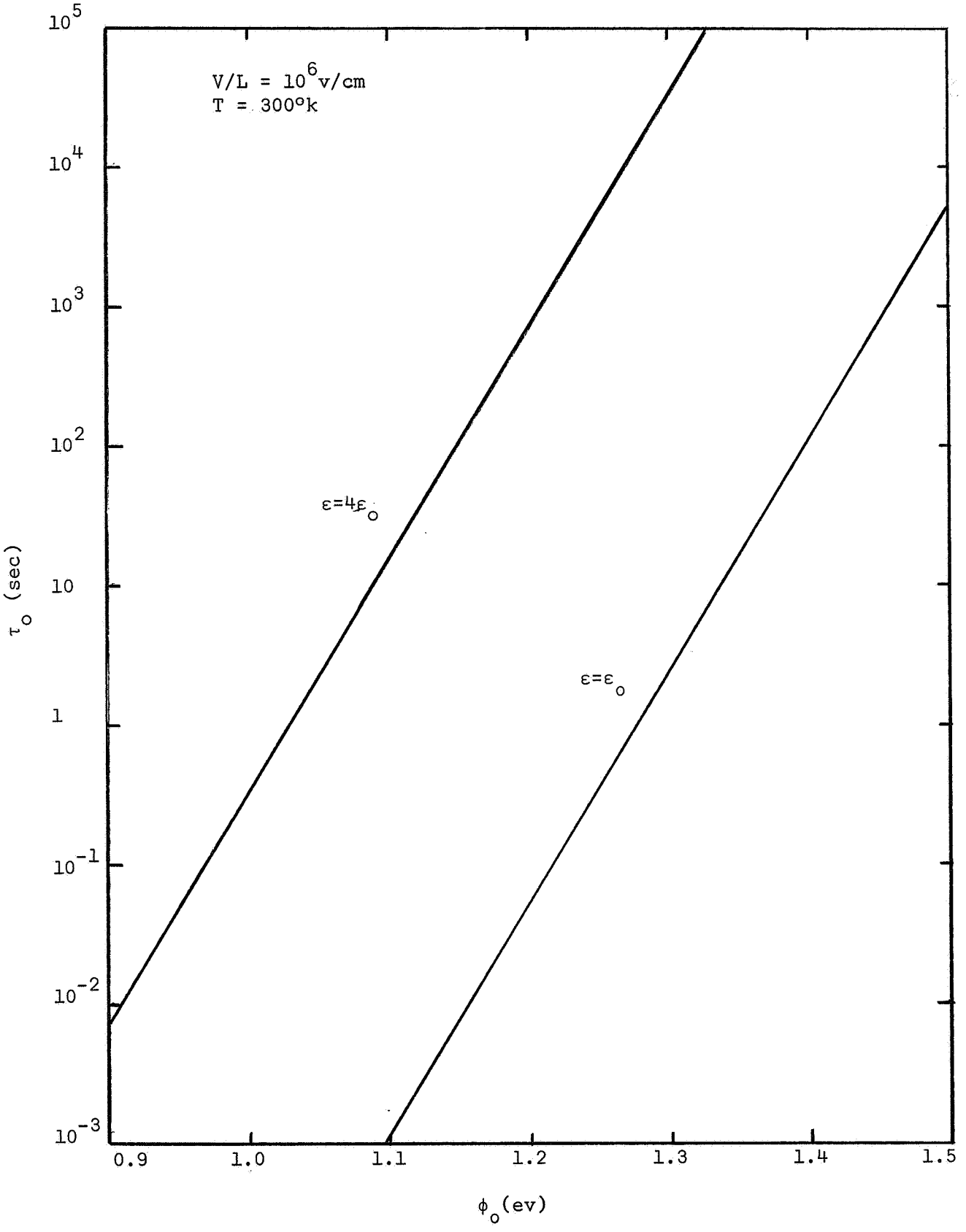


Figure 21. Time constant τ_o as a function of barrier height at 300°k

One way of minimizing the electronic instability due to Schottky injection is to use an insulator which has a large barrier height between the insulator and semiconductor for both hole and electron injection. A large barrier means that τ_o becomes very large, and Schottky injection may be negligable unless one applies a bias for extremely long periods of time. Suppose for example that one wishes to have τ_o larger than 10^5 sec which is just less than two days. Figure 22 shows the required barrier height as a function of temperature. At 300° C it is seen to require a barrier height of between 2.5 and 3.0 ev. Considering that this is only for one type of carrier, one must have a total insulator barrier height of from 6 to 7 ev in order to have an MIS structure which does not show significant electronic instability at temperatures of 300°C and for times on the order of 10^5 sec. This illustrates the large barriers required at high temperatures to reduce Schottky barrier injection to a negligable effect.

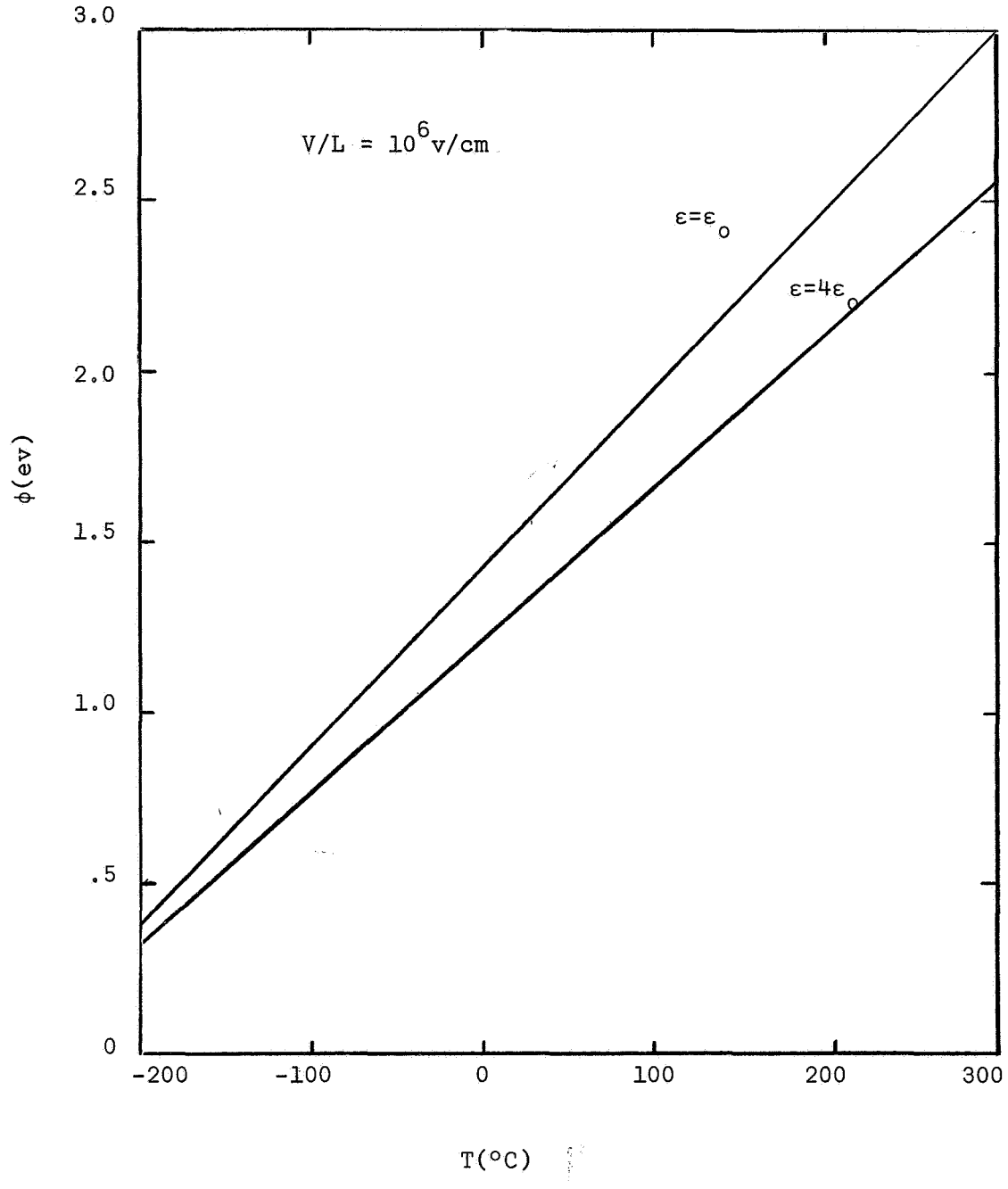


Figure 22. Barrier height required to make $\tau_o = 10^5$ sec as a function of temperature.

EXPERIMENTAL TECHNIQUES AND RESULTS

This section discusses the experimental techniques, the experimental system used for MIS charge injection studies, and the requirements this system must satisfy. The system is basically a standard capacitance bridge with auxiliary equipment which allows continuous, rapid measurement of capacitance versus voltage as opposed to point by point measurement. Speed and other limitations as well as some suggestions for improvement of the system are also considered.

In order to study MIS charge injection the shift in flat-band voltage with time must be accurately known. This information can be obtained from plotting capacitance versus voltage and measuring the shift in flat-band voltage between successive curves. The C-V curves are assumed to shift parallel to each other for a fast C-V bias sweep as previously discussed, so the flat-band voltage shift measurement can be made at any convenient point along the curves. The C-V measuring system under consideration allows for automatic display of these C-V curves and hence display of the flat band voltage shift.

The requirements that the experimental system must meet have been implicitly set forth in section 2. These requirements can be restated as follows:

1. The system must display the shift in flat-band voltage.

2. It must be possible to obtain "fast" C-V curves,i.e., voltage sweep times as fast as 50 milliseconds.

3. The sweep voltage applied across the MIS capacitor must be linear, and the bias voltage must be stable.

4. The temperature of the MIS device is a parameter and must be controllable and stable.

These conditions can be considered in more detail with reference to the specific system used to obtain the experimental information appearing in this report. Figure 23 shows diagramatically the particular system used. The core of this automatic C-V display system is the General Radio Model 716-C Capacitance Bridge and the Tektronic Model 547 Oscilloscope. The capacitance bridge is used to sense the variation in MIS capacitance which is consequently displayed on the oscilloscope vertical axis. The oscilloscope horizontal axis is controlled by the internally generated sawtooth which is also used externally to linearly vary the bias across the MIS capacitor. The speed of the C-V trace is controlled by setting the horizontal display time.

Since a positive to negative range of voltages is needed to obtain the C-V curves, and the oscilloscope generates a positive ramp only, a DC offset is obtained by using a battery and a resistive divider. This offset voltage is also used to bias the MIS device for the times between fast C-V traces, so it must be stable because slight variations in it will show up as an additional erroneous shift in the flat-band voltage. Stability has been acheived by using several batteries in parallel with a zener diode which has a capacitor across it to reduce noise.

Temperature control is obtained by fastening the MIS device, which is mounted on a TO-5 Header and sealed in a inert atmosphere (argon), to an aluminum block which is located inside an environmental chamber manufactured by Hafstrom Technical Products, Inc. model 700WS. Temperature stability is not too critical since the maximum variation is a few degrees Kelvin out of approximately several hundred degrees. Percentage wise the variation is small.

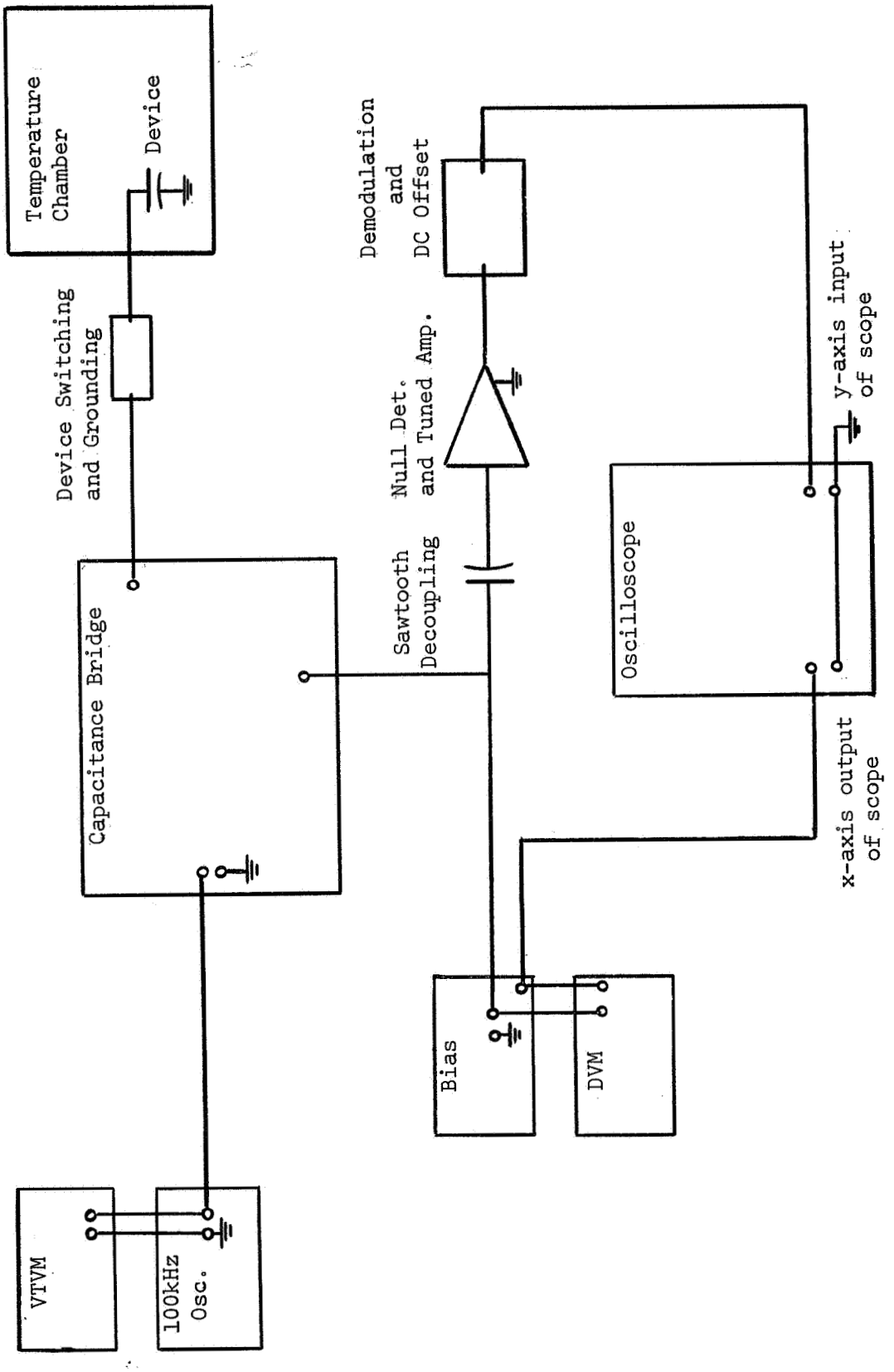


Figure 23. Sketch of C-V measuring equipment

Now that the requirements which any fast C-V system must meet have been set forth and explained in terms of a particular system the task of considering this particular system in more detail remains. The detail concerns the equipment auxiliary to the core components the capacitance bridge and the oscilloscope. An important component in the system which requires no explanation for its presence is the Hewlett-Packard Model 200CD Wide Range Oscillator. It is used to supply the 100kHz error sensing signal to the generator terminals of the capacitance bridge. A Hewlett-Packard model 400A VTVM monitors the RMS output voltage from the 100kHz oscillator. The voltage is set so that 25 millivolts RMS appears at the generator terminals of the capacitance bridge.

Biasing of the device has been mentioned briefly, but further consideration is necessary. The battery and resistive divider network discussed above is in series with the sawtooth voltage generated by the oscilloscope, and these two are essentially in parallel with the MIS device. Unless the oscilloscope is triggered externally there is no sawtooth, and the bias voltage alone appears across the device. This bias voltage must have a positive or negative polarity with respect to the metal electrode depending on whether electron or hole injection into the insulator is to be studied. In order to facilitate this bias polarity reversal a double-pole, double-throw switch was installed between the device terminals on the bridge and the device located in the environmental chamber. This switch reverses the metal and semiconductor electrodes which has the same effect as reversing the polarity of the bias voltage. Contained in the box with the reversing switch are two wafer switches which allow one to short the metal electrode to the semiconductor electrode of one of two devices on a TO-5 header while switching the other device into the C-V measuring system. Also, these switches are used to ground a device after data has been taken at a given temperature over a certain time period.

To determine when the capacitance bridge is balanced a General Radio type 1232-A Null Detector and Tuned Amplifier is used in the system. To detect the output from the null detector—tuned amplifier, as the changing device capacitance unbalances the capacitance bridge, a low loss diode detector is inserted between the null detector—tuned amplifier and the vertical input of the oscilloscope. The detector consists of an emitter follower which presents a high impedance load to the null detector—tuned amplifier and a low impedance source to the diode detector and filter which demodulates the output signal from the bridge yielding a voltage which is proportional to the change in capacitance of the MIS device. The tuned amplifier must have a very high voltage gain (approximately 10^5) in order to detect the small error signal from the capacitance bridge generated by the slight change in MIS capacitance. Because the tuned amplifier has such a high voltage gain the sawtooth generated by the oscilloscope can easily over-drive it. Therefore a 50pf capacitor is used to couple the 100kHz error signal to the tuned amplifier and to decouple the sawtooth.

To use the system, a device is placed inside the environmental chamber and heated or cooled to the desired temperature. During this time the metal electrode is shorted to the semiconductor electrode, and power is applied to all equipment. Initially the 100kHz oscillator output voltage is set for 25mv across the bridge, the bias voltage is set at 25 volts using the digital voltmeter, and the sawtooth linearity and amplitude is checked by observing it on the oscilloscope after connecting a probe from the device terminals of the bridge. The bias is set to vary over the range from plus to minus 25 volts. Since the horizontal axis of the oscilloscope is now calibrated at 5v/cm, the shift in flat-band voltage can be determined directly in volts. After the initial adjustments have been made a MIS device is switched into the C-V system.

Bias is applied to the device, and the bridge is nulled. A few initial C-V curves are made to allow adjustment of the tuned amplifier gain and the oscilloscope vertical amplifier gain, so that the C-V curve covers the entire face of the oscilloscope. The device is shorted again for several hours to allow the charge in the insulator to return to its equilibrium value. Then the system is ready for data collection.

Typical procedure for studying charge injection in a particular device was as follows: the system was readied as above; the MIS device was unshorted; the polaroid camera lens was opened; bias was applied, a stop watch was started, and the oscilloscope was triggered externally, all at the same instant of time, to yield an initial (supposedly zero time) curve. The camera lens was then shut. The bias remained applied and the stop watch continued to run for 5 seconds at which time the oscilloscope was again triggered to engrave another C-V curve on the polaroid negative. Since multiplying a number by some factor, two in this case, moves one linearly along a logarithmic scale, C-V curves were also taken at 10, 20, 40, 80, 160, 320, and 640 seconds and at 1.3, 2.6, and 5.2 times 10^3 and 1, 2, 4, 8, times 10^4 seconds. Also, choosing these times left little room for error since the same points were always used on the time axis of the semilog plot. Since the shift in flat-band voltage is directly related to the injected charge density (see equation 5) a plot of injected charge density versus the logarithm of time was obtained. Of course included in this charge density is any charge trapped by surface states at the insulator-semiconductor interface.

Total time required to obtain data at one temperature and for one type of electronic charge (hole or electron) injection was about 24 hours. The same precedure was followed at the same temperature for injection of the other

type of charge, and then the process was repeated at other temperatures. The temperatures generally used were 0, 20, 40, 60, 80, and 100 degrees centigrade. Sometimes additional information could be obtained at -25°C. After 24 hours under bias a device was shorted for approximately 48 hours to allow the injected charge to get out of the insulator before further study could be undertaken.

The accuracy of the system can be discussed in terms of the possible sources of error within it. It has been tacitly assumed up to this point that the quality factor, Q, of the MIS capacitor is greater than 10. With this assumption the unbalancing of the capacitance bridge is attributable to the variation of MIS capacitance only, as opposed to variation in parallel resistance. To verify the validity of this assumption capacitance and resistance versus voltage were plotted point by point for several devices, and the parallel resistance was observed to be immeasurably large. Another source of error was the noise generated by the high gain tuned amplifier. Minimum amplifier gain was used to reduce the noise to an acceptable level, meaning the C-V curve on the oscilloscope face approached as near as possible the ideal shape. A third source of error can be attributed to the fact that three voltages-the bias, the sawtooth, and the 100kHz error signal-appeared across the device under test. These voltages created an uncertainty as to exactly where each C-V trace started on the voltage axis. These errors should occur randomly for various C-V curves, however. An additional, non-random error can occur if the bias voltage drifts in one direction (normally downward). A small variation of one-tenth of a volt out of 25 volts causes an apparent shift in the C-V curve which can be as great as the flat-band voltage shift between curves. Obviously this error can be avoided by keeping the bias supply voltage constant. The bias supply must also be noise free due to the high sensitivity of the null detector and tuned amplifier.

Other possible error sources come from the environmental chamber and capacitance bridge. The environmental chamber specifications stipulate a ±0.1°C temperature control capability. Control of about ±1°C was actually observed. The accuracy of the capacitance bridge is specified as ±(0.1%+1pf) which has been confirmed through the use of a precision capacitor. The overall accuracy and linearity of the system was also checked with a General Radio type 1422-MD precision capacitor and proved acceptable.

In conclusion, some comments about speed of operation and about general ways to improve the system are in order. The present system operates with a total bias sweep time of 50 ms. (Oscilloscope horizontal display time is set at 5ms/cm.) The total bias sweep time could be as fast as 100 μs with some loss in linearity of the external sawtooth voltage which is applied to the MIS device. Also the problem of coupling the sawtooth to the null detector becomes more critical. The source impedances of the bias supply, battery and oscilloscope with respective resistive dividers, and the null detector-tuned amplifier coupling capacitor together, determine how much of the sawtooth is coupled into the detector circuits as error. These impedances would have to be readjusted for higher sweep rates. Varying the bias at a high rate would also require a higher error signal frequency as discussed in Chapter 2. Greater bias sweep rates are desirable since they enhance the accuracy of short time data (less than one second). Using differential techniques to keep the sawtooth out of the tuned amplifier and using a high gain tuned amplifier optimized as an amplifier instead of a null detector could add considerably to system performance.

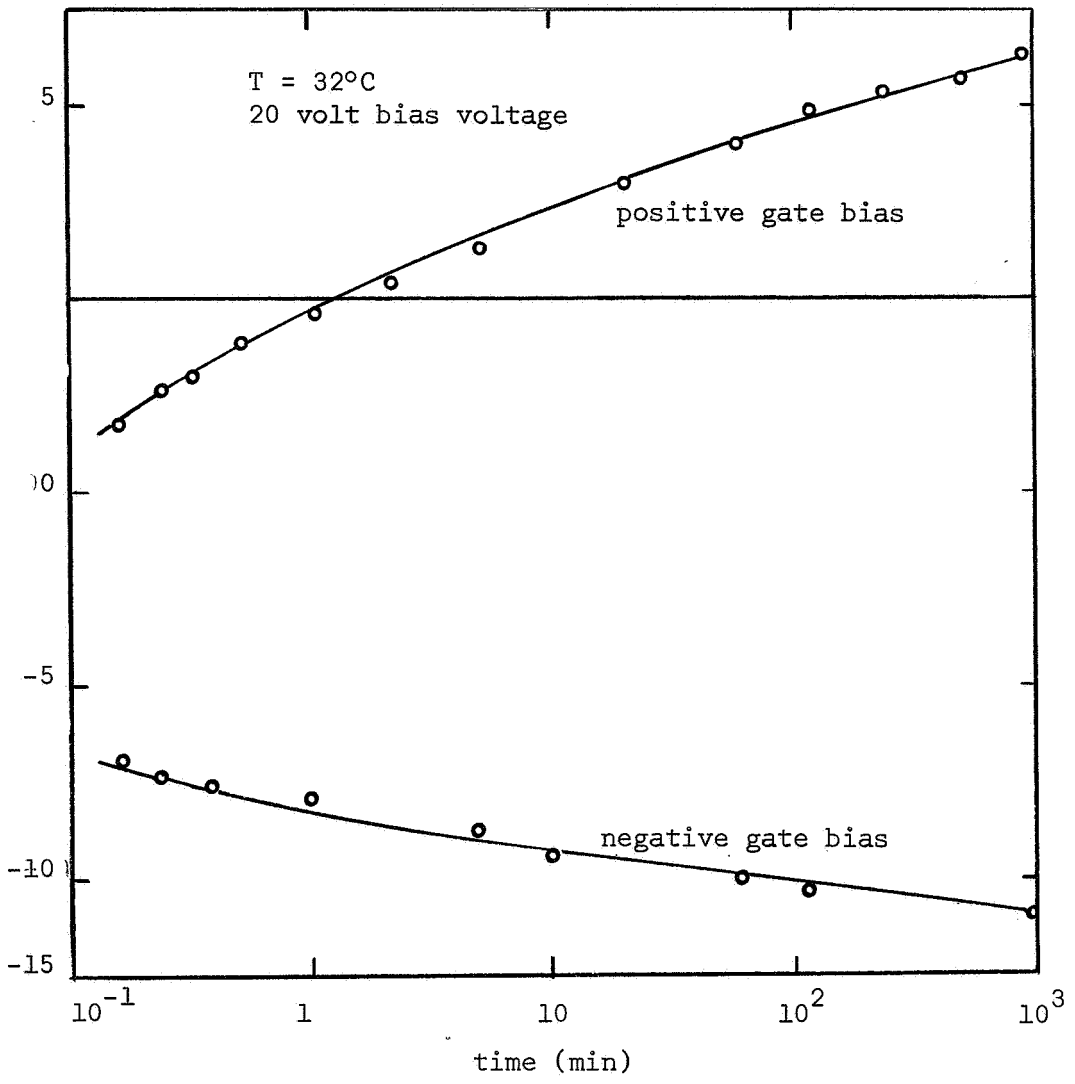


Figure 24. Typical shift in flat-band voltage with time under positive and negative bias for Si_3N_4 devices

Typical changes in flat-band voltage for the silicon nitride devices are shown in Figure 24 for a device at room temperature. To obtain the experimental data the device was biased in this case at a constant voltage of either +20 volts or -20 volts. Fast C-V sweeps (50 msec from -20 to +20 volts) were taken at the time intervals shown in the figure. Assuming that the sweep is sufficiently fast not to disturb the insulator charge appreciably, the changes in flat band voltage then correspond to changes in insulator charge. Several important features are noted from the data. First a negative bias causes V_{FB} to shift in the negative voltage direction

indicating an increase in positive charge near the insulator semiconductor interface. A positive bias produces a shift toward larger positive voltages indicating an increase in negative charge near the semiconductor insulator interface. It is noted that the flat-band voltage changes from negative to positive values indicating the dominance of negative charge after long positive gate bias. These changes are in the opposite direction to those normally observed on SiO_2 devices and can only be explained by an electronic motion as discussed in the previous section and cannot be explained by ion motion within the insulator.

A second major feature of the data is the extremely long time nature of the phenomena. As the data indicates, significant changes in flat-band voltage are occuring in times less than a few seconds, and at the other extreme there is as yet no tendency for saturation of the flat-band voltage changes even after many hours. As discussed in the previous section it is difficult to distinguish absolutely between charge injection into the bulk of the insulator and interface state charge changes. It is believed, however, that the extremely long time nature of the phenomena indicates a bulk injection effect. Changes in interface state density would be expected to be exponentially related to time and not to behave in the manner shown in Figure 24.

The above major features have been consistently observed on many samples and at many different temperatures. Typically the observed changes at room temperature were such that significant changes in the charge occured in times of less than one second. This makes it difficult to observe at room temperature the initial changes in flat-band voltage following the application of a voltage pulse. The phenomena can be slowed down somewhat by going to reduced temperatures. Typical data for a device at 0°C is shown in Figures 25 and 26. The change in flat-band voltage has

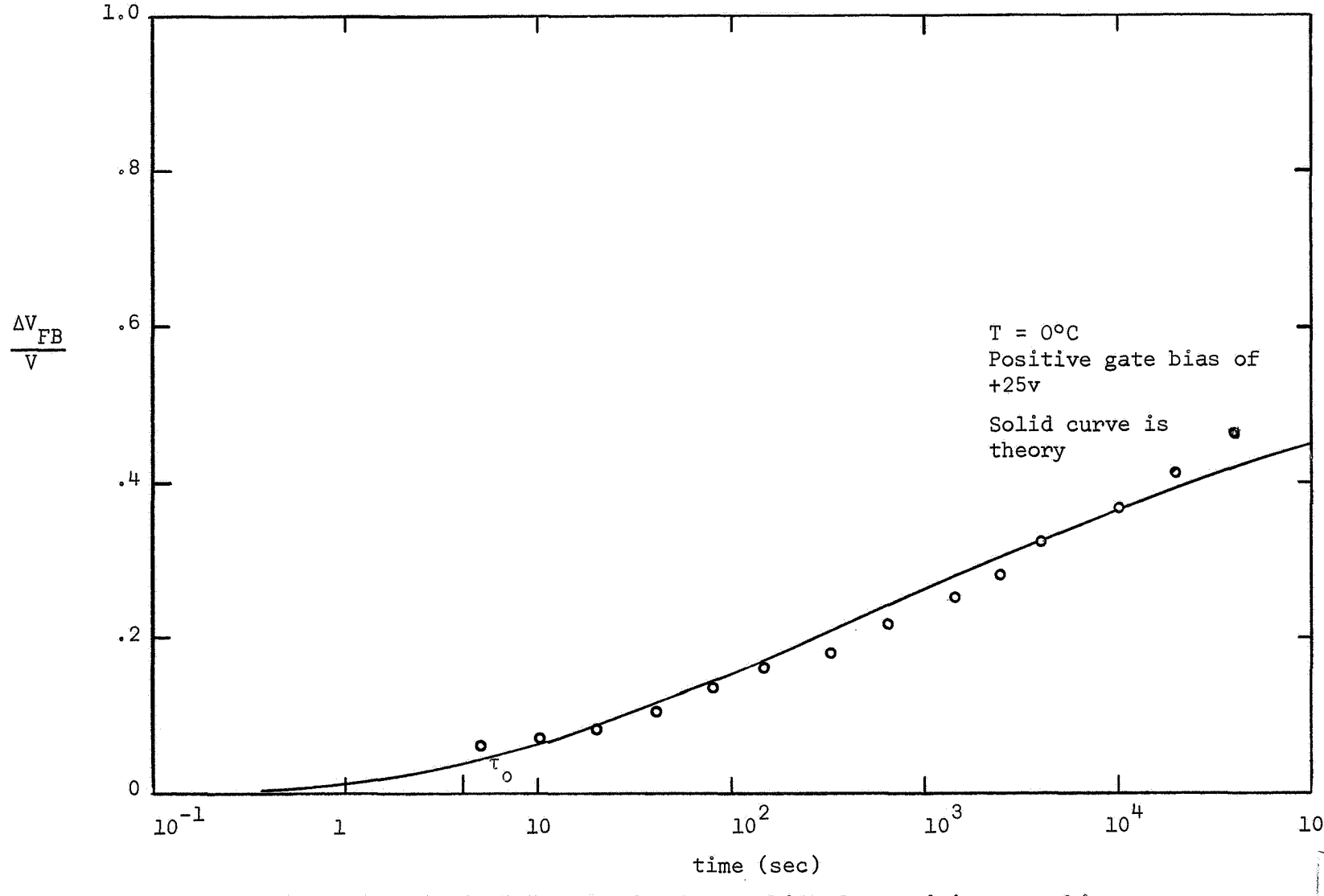


Figure 25. Typical Flat-band voltage shift for positive gate bias.

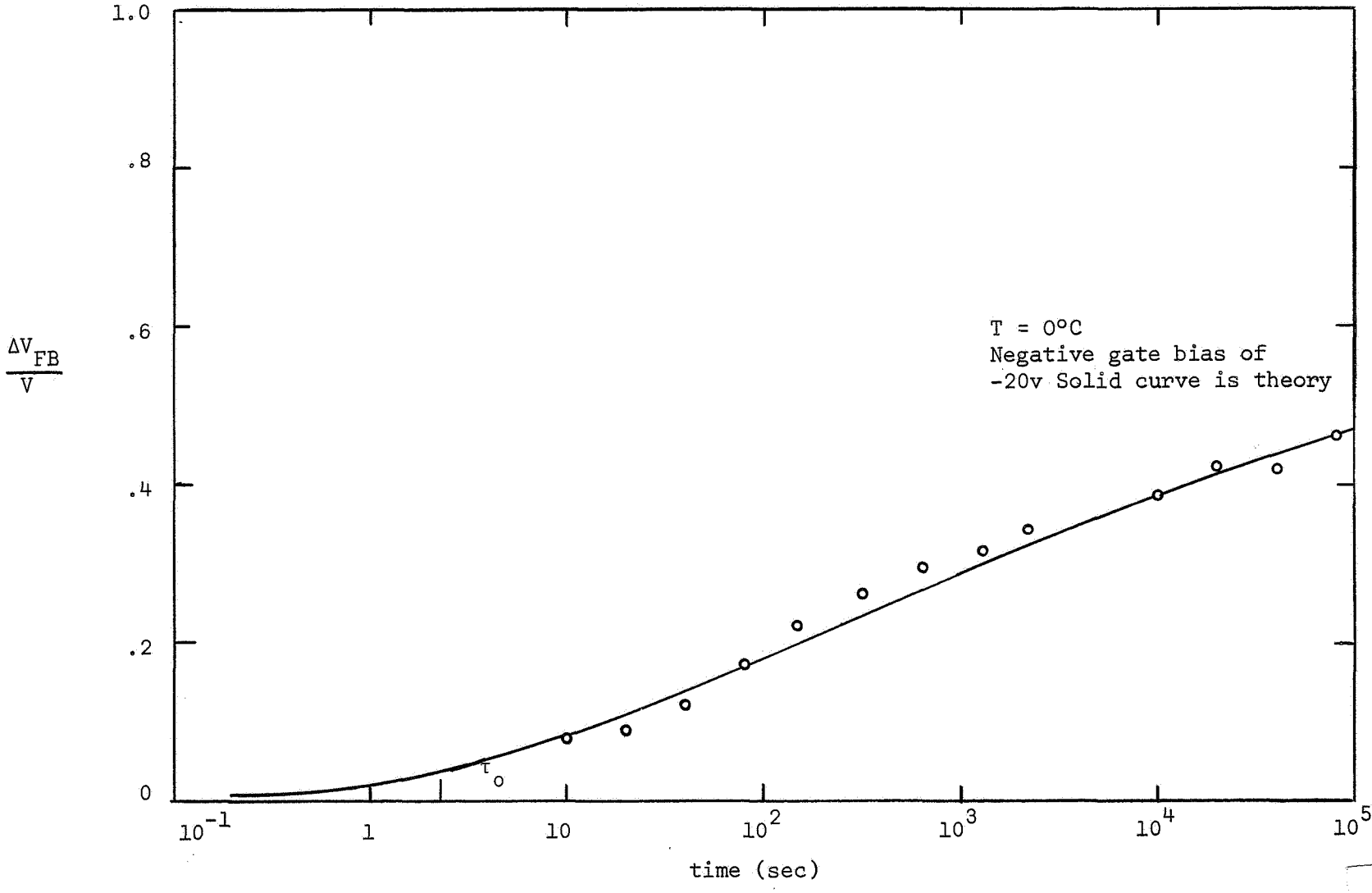


Figure 26. Typical flat-band voltage shift for negative gate bias

been normalized with respect to the applied voltage. The solid lines in the figures are theoretical curves similar to those shown in Figure 18. The corresponding value of τ_o for both electron and hole injection is indicated in the figures. In both figures the solid curves correspond to Z_o values of approximately 36. The theoretical value calculated using the applied voltage and the insulator thickness is 29.3 which is about 25% smaller than the value needed to give the best fit to the experimental data. This means that the initial barrier lowering required to give the theoretical curves is slightly larger than the initial barrier lowering calculated using the applied voltage and average insulator thickness. The exact reason for this is not known. It may be due to the initial insulator charge which is not considered in the theoretical model but which does make a significant contribution to the total insulator charge. It could also be due to a nonuniform thickness of the insulator film.

From the values of τ_o given in Figures 25 and 26 maximum estimates of the barrier for both electrons and holes can be obtained using the model of the previous section. These calculations give the values

$$\phi_{no} \simeq 1.53\text{ev},$$

$$\phi_{po} \simeq 1.51\text{ev}. \tag{51}$$

These values were calculated on the assumption that the injected charge is trapped close to the insulator-semiconductor interface. If this is not the case then the barriers will be even lower than those calculated above. The above values indicate a total barrier height for the silicon nitride film of

$$E_{gi} \simeq 4.14\text{ev}. \tag{52}$$

This value is close to the value of 4.5ev reported by Gray [24] as

obtained by optical measurements on silicon nitride. This agreement provides additional support for the Schottky barrier injection model as proposed in this work.

This data shown in Figures 25 and 26 indicate almost completely symmetrical behavior for both positive and negative bias with an almost identical barrier for both types of injection. Many devices were found to exhibit an unsymmetrical behavior with respect to positive and negative bias. Data for such a device are shown in Figures 27 and 28. It is seen that for positive bias, times longer than 10^4 sec are required before any appreciable shift in the flat-band voltage is observed. On the other hand for negative bias the change is very rapid and has essentially saturated for times larger than 10^3 sec. This type of behavior indicates a larger barrier for electron injection than for hole injection. The approximate values of τ_o are indicated in the figures and these lead to the calculated barrier heights of

$$\begin{aligned} \phi_{no} &\simeq 1.71\text{ev}, \\ \phi_{po} &\simeq 1.53\text{ev}, \end{aligned} \tag{53}$$

and thus a total band gap for the silicon nitride of

$$E_{gi} \simeq 4.34 \text{ ev}. \tag{54}$$

These slight differences in barrier height and in total band gap for the silicon nitride films are not very surprising when it is recalled that a fairly wide range of deposition parameters (i.e silane-to-ammonia ratios) were used in depositing the films. A study of the effect of the deposition parameters on the barrier heights would be an interesting study. It is also interesting to note that the approximately four orders of magnitude time difference in the response for positive and negative bias is accounted for by barrier height differences for hole and electron injection of only 0.2ev.

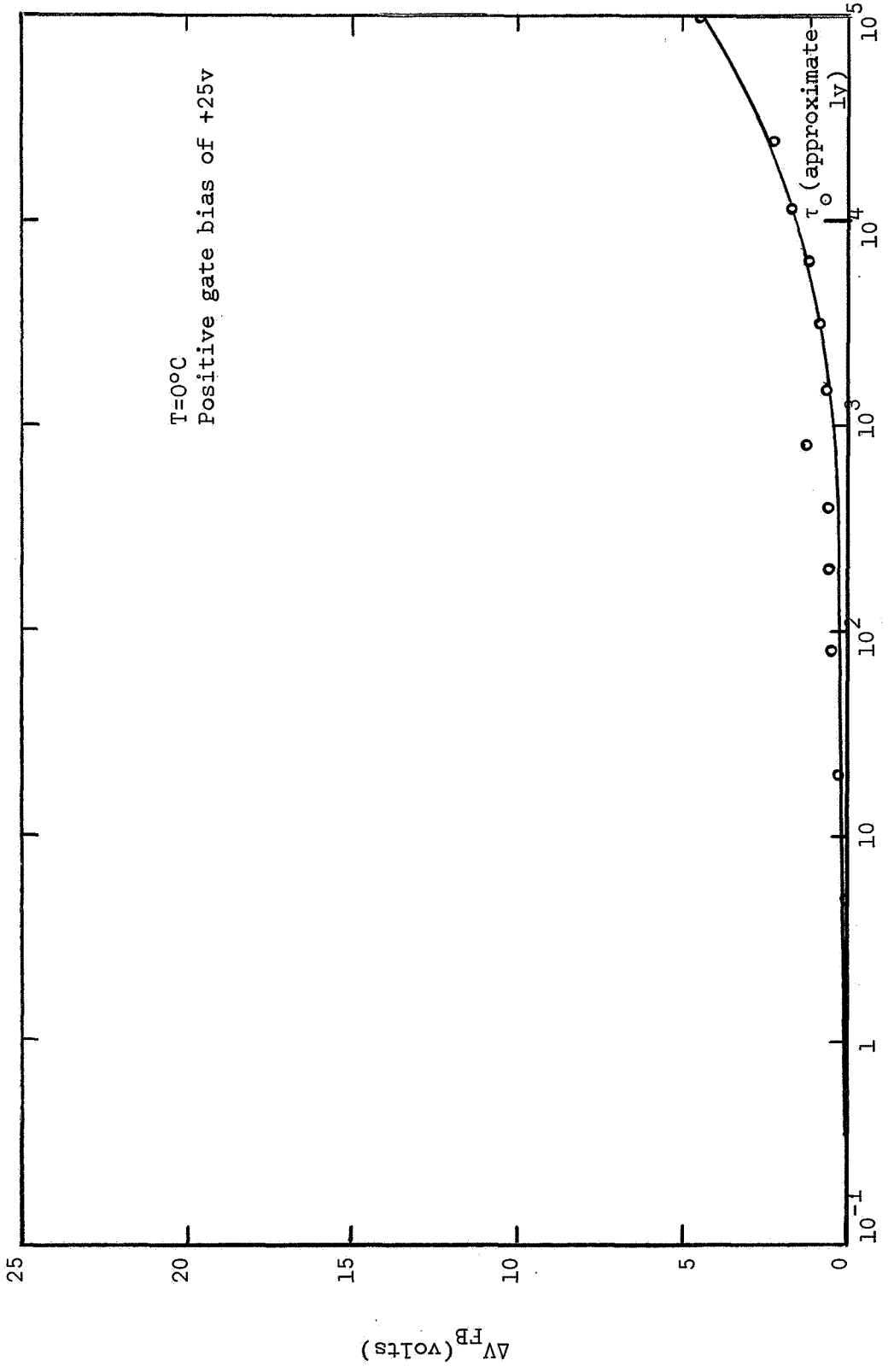


Figure 27. Flat-band voltage shift for positive gate bias for an unsymmetrical device.

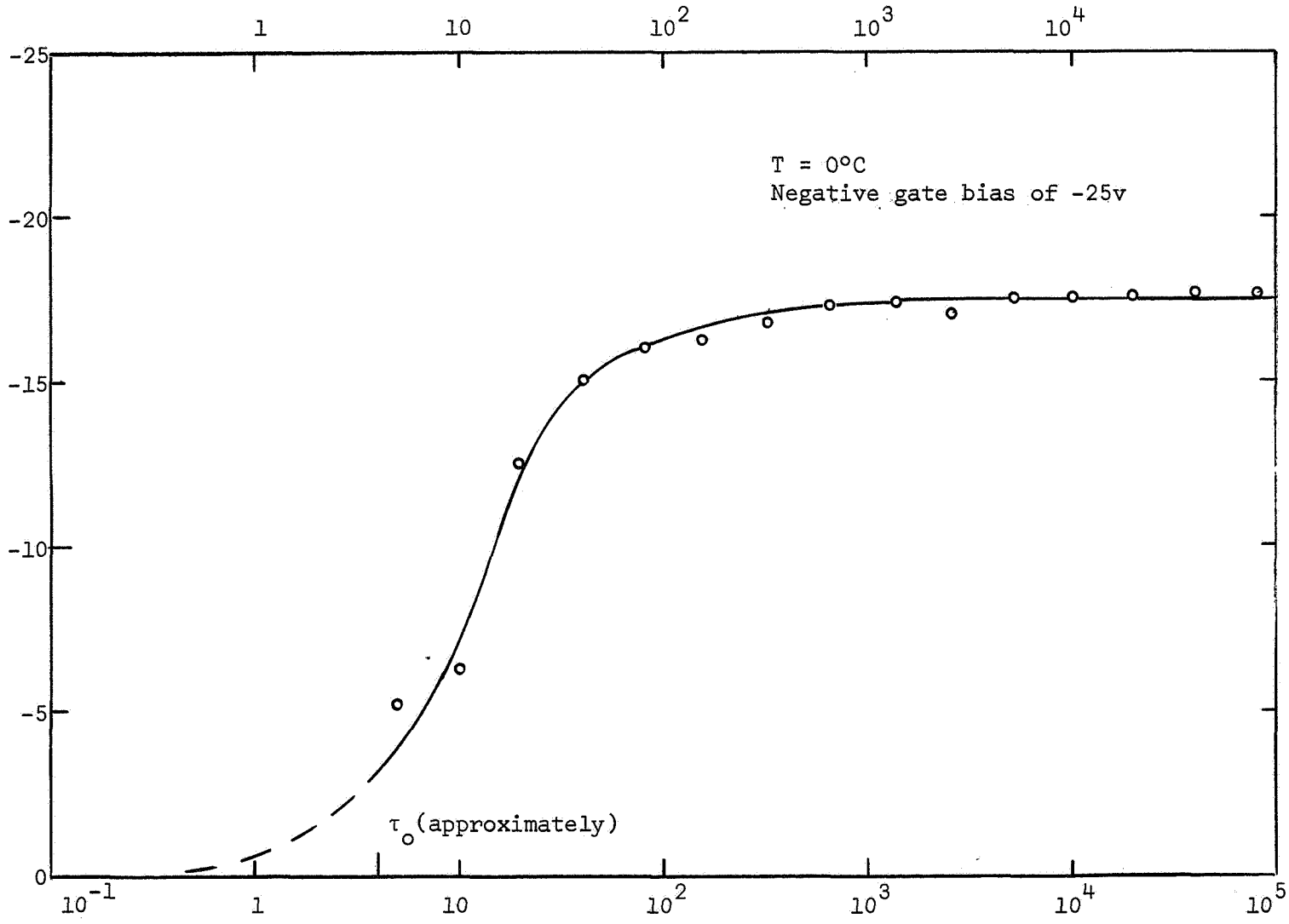


Figure 28. Flat-band voltage shift for negative bias for an unsymmetrical device.

The data in Figure 28 also indicates the saturation of the flat-band voltage shift at about 17.5 volts for an applied voltage step of 25 volts. A qualitative explanation of this is given in the previous section in connection with Figure 19. This is to be expected on all devices but was rarely observed because of the long time required to observe this effect on most devices.

The data shown in the previous figures is typical of that obtained on a large number of devices. Practically all devices exhibited a calculated total silicon nitride band gap of about 4.2 ev with particular devices ranging to as much as 0.2 ev on either side of this value.

Occasionally some devices were found to exhibit erratic behavior. Data for such a device are shown in Figure 29. It appears that the injected charge is rapidly being compensated in some manner when the discontinuous behavior occurs. This compensation may be due to high field breakdown in the nitride insulator. Some devices were also cooled to liquid nitrogen temperature and found to exhibit erratic behavior following this low temperature. The physical origin of this erratic type of behavior is not completely understood and has not been extensively investigated in this work.

In addition to the C-V measurements discussed above, transient current measurements on the silicon nitride devices were also attempted. The gate current should give an indication of the depth to which the injected charges move in the insulator before becoming trapped. If the total charge flowing to the gate is considerably less than the charge build-up within the insulator, then the charge must be trapped close to the interface. On the other hand if the gate charge flow is considerably larger than the insulator charge build-up, the bulk of the charge flow must be completely through the insulator with little trapping. Current measurements were

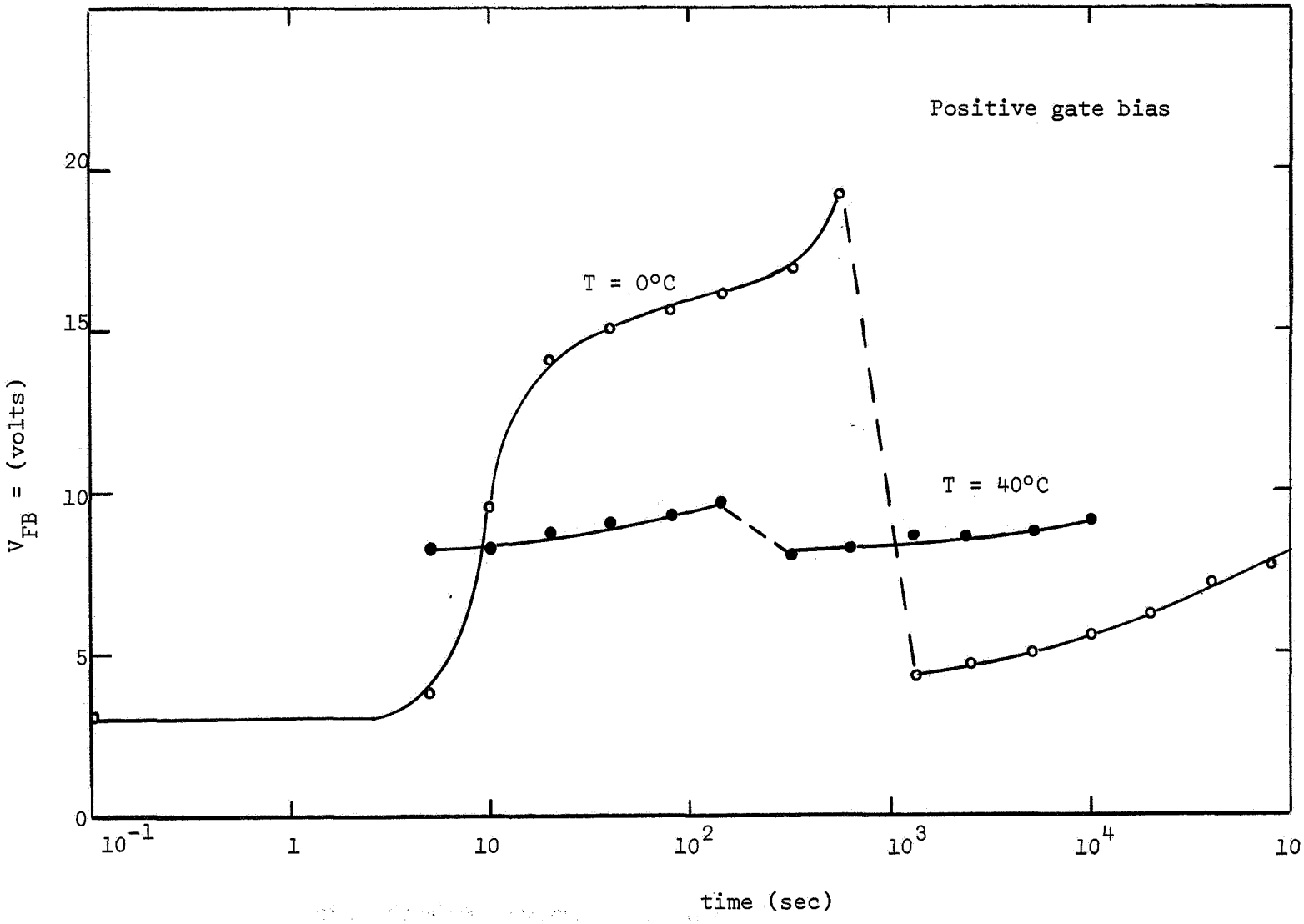


Figure 29. Erratic behavior observed on some devices.

made with a Keithley model 610B electrometer in series with the device under the voltage bias experiments. No correlation was found between the measured current and the change in flat-band voltage. Typically the current remained constant at a value in the neighborhood of 10^{-7} to 10^{-8} amp during the entire measurement. These are considerably larger currents than those needed to explain the shifts in flat-band voltage. It is believed that the observed currents were due to surface leakage and not to a bulk current flow. This would explain the constant value of measured current. Also it was observed that the value of current could be changed by blowing on the device. This is another good indication that the observed current was due to surface leakage.

5. DISCUSSION AND CONCLUSIONS

The present work has been concerned mainly with one particular type of instability in MIS structures. This is the electronic type of instability which is due to Schottky barrier injection of electrons and holes into the insulator and the subsequent trapping of these carriers in the insulator. A general discussion has been presented of all types of MIS instabilities and a detailed discussion of Schottky barrier injection.

The experimental data for silicon nitride insulating films agrees pretty well with the theoretical model for Schottky barrier injection. The more important features of the charge instability in silicon nitride films are the opposite direction of the changes in insulator charge from that of silicon dioxide and the very long time nature of the phenomena. The shift in flat-band voltage of an MIS capacitor following the application of a bias voltage is found both theoretically and experimentally to depend essentially on ln(t) over a large time interval. This is a type of time dependence rarely encountered in nature and requires special care in making measurements. The observed changes were found to occur over more than six orders of magnitude in time. This makes data taking of such an effect very difficult because one must be able to handle both short times in the millisecond range and long times on the order of days. Drift in the equipment becomes a problem for very long time measurements.

From the experimental measurements and the theoretical model, barrier heights for electron and hole injection into the insulator from the silicon have been estimated as well as the total band-gap in the silicon nitride insulator. The barriers for holes and electrons have been found to be about 1.5ev to 2.0ev. The barrier for hole injection was typically found

to be a few tenths of an ev smaller than the barrier for electron injection. Some devices were observed, however, to have approximately equal barriers for both types of carriers. Variations in the individual electron and hole barriers tended to be somewhat larger than the variations in the total band-gap of the silicon nitride which has been estimated to be 4.2ev ± 0.2ev. Some of the observed differences in energy barriers from device to device are probably due to differences in the deposition parameters.

The work described in the report does not directly involve radiation effects on surface properties. This work, however, grew out of early attempts to study gamma irradiation effects on silicon nitride capacitors. The initial irradiations gave inconclusive results because of the large instability present in these devices. It was recognized that a more complete understanding was needed of the instability in silicon nitride before meaningful irradiation work could be undertaken. It is believed that this work has now provided a consistent and first order explanation of the electronic type of instability present in silicon nitride.

A very important problem in connection with MIS devices, including silicon dioxide devices, is to decrease the sensitivity to irradiation. Much effort is presently being exerted by many groups on this problem. The present work sheds important light on the direction in which this work must go. It is now generally recognized that the sensitivity of silicon dioxide MOS devices to irradiation is due to the large assymmetry in the trapping of electrons and holes. Created electrons are able to get out of the silicon dioxide while the holes become trapped almost immediately at the point where they are created. Short of creating a

trap free insulator which does not appear to be very likely, the only solution to this problem is to use an insulator in which both electrons and holes are very rapidly trapped after being created by irradiation. The use of silicon nitride and various other deposited insulators such as aluminum oxide and deposited SiO_2 appear to offer advantages over thermally grown SiO_2. In addition ion motion in silicon nitride and aluminum oxide is greatly reduced over that in silicon dioxide. The present work shows, however, that electronic injection into the insulator can be a very real problem with silicon nitride (it may also be a problem with aluminum oxide). As discussed in this report one must have an insulator with a total band gap in the neighborhood of 7ev in order to eliminate Schottky barrier injection at a temperature of 300°C. This rules out many insulators including silicon nitride for use directly on silicon.

Thermally grown silicon dioxide has been found to have the required band-gap (on the order of 8ev) to minimize the electronic type of Schottky barrier injection. This may very likely prove to be the best insulator for the silicon-insulator interface. A thin layer of SiO_2 followed by other insulators such as silicon nitride or aluminum oxide are likely to lead to the most insensitive MIS devices. Some initial work has been done in this area using silicon nitride insulators with a very thin layer of thermally grown oxide near the silicon, and the results do indicate a decreased irradiation sensitivity. Vacuum evaporated SiO and deposited SiO_2 may also have desirable properties if the ion problem can be eliminated in these materials.

REFERENCES

1. An extensive bibliography of work on M-I-S structures is given by the following reference: Earl S. Schlegel, "A Bibliography of Metal-Insulator-Semiconductor studies", IEEE Trans. Electron Devices, vol. ED-14, pp. 728-749, 1967.

2. J. P. Mitchell and D. K. Wilson, "Surface effects of radiation on semiconductor devices," Bell Sys. Tech. J., vol. 46, pp.1-80, 1967.

3. Y. Miura, "Effect of orientation on surface charge density at silicon-silicon dioxide interface," Japan J. Appl. Phys., Vol. 4, pp. 958-961, 1965.

4. J. S. Logan and D. R. Kerr, "Migration rates of alkali ions in SiO_2 Films," IEEE Solid-State Device Research Conf., Princeton, N. J., June 1965.

5. A. B. Kuper, C. J. Slabinski, and E. Yon, "Positive-and negative-ion motion in thermal oxide on silicon by radiochemical and MOS analysis," RADC Ser. in Reliability, Physics of Failure in Electronics, vol. 5, pp. 232-243, 1967.

6. E. Yon, W. H. Ko, and A. B. Kuper, "Sodium distribution in thermal oxide on silicon by radiochemical and MOS analysis," IEEE Trans. Electron Devices, vol. ED-13, pp. 276-280, 1966.

7. S. R. Hofstein, "Stabilization of MOS Devices", Solid State Electronics, vol. 10, pp. 657-570, 1967.

8. J. V. Dalton, "Sodium drift and diffusion in silicon nitride films," 1966 Spring Meeting of Electrochem. Soc., Cleveland, Ohio, Recent News Paper, Abstract 23.

9. H. Lawrence and C. Simpson, "Stability properties of nitride films on silicon," 1966 Fall Meeting of Electrochem. Soc., Philadelphis, Pa., Abstract 159.

10. J. R. Szedon, T. L. Chu, and G. A. Gruber,"Charge instability in metal-silicon nitride-silicon structures," IEEE Solid-State Devices Research Conf., Evanston, Ill., June 1966.

11. H. E. Nigh, J. Stach, and R. M. Jacobs, "A sealed gate IGFET," IEEE Solid-State Devices Research Conf., Santa Barbara, Calif., June, 1967.

12. C. L. Hutchins, "Charge Transients in Aluminum-Silicon Nitride-Silicon Capacitors," Ph.D. Thesis, Electrical Engineering Dept., N. C. State University, Raleigh, North Carolina, 1968 (N. C. State University, Semiconductor Device Laboratory Report SDL-8-588-1).

13. C. L. Hutchins and R. W. Lade, "Charge Storage in Metal-Silicon Nitride-Silicon Capacitors, Proc. IEEE, vol. 55, p. 1494, 1967.

14. R. J. Mattauch, "A Study of the Effects of Co^{60} γ-Radiation on Steam-Grown SiO_2 MOS Structures, " Ph.D. Thesis, Electrical Engineering Dept., N. C. State University, Raleigh, N. C., 1966 (N. C. State University, Semiconductor Device Laboratory Report SDL-5-588-1).

15. R. J. Mattauch and R. W. Lade, "Surface State Density Variations on MOS Structures Due to Gamma Radiation," Proc. IEEE, vol. 53, p. 1748, 1965.

16. M. A. Littlejohn, "Influence of Co^{60} Gamma Irradiation on the Bulk and Surface Recombination Rates in Silicon," Ph.D. Thesis, Electrical Engineering Dept., N. C. State University, Raleigh, North Carolina, 1967 (N.C. State University, Semiconductor Device Laboratory Report SDL-6-588-1).

17. A. S. Grove, Physics and Technology of Semiconductor Devices, John Wiley and Sons, Inc. New York, 1967.

18. A. Goetzberger, "Ideal MOS Curves for Silicon", Bell System Tech. J., vol. XLV, pp. 1097-1122, 1966.

19. D. R. Kerr, "Effect of Temperature and Bias on Glass-Silicon Interfaces," IBM Journal of Res. and Dev. , vol. 8, pp. 385-393, 1964.

20. B. E. Deal, M.Sklar, A. S. Grove, and E. H. Snow, "Characteristics of the Surface-State Charge (Q_{ss}) of Thermally Oxidized Silicon", J. Electrochem. Soc., vol. 114, pp. 266-274, 1967.

21. F. P. Heiman and G. Warfield, "The Effects of Oxide Traps on the MOS Capacitance", IEEE Trans. Electron Devices, vol. ED-12, pp. 167-178, 1965.

22. A. K. Jonscher, "Electronic Properties of Amorphous Dielectric Films", Thin Solid Films, vol. 1, pp. 213-234, 1967.

23. R. M. Hill, "Single Carrier Transport in Thin Dielectric Films", Thin Solid Films, vol. 1, pp. 39-68, 1967

24. S. N. Levine, Quantum Physics of Electronics, The Macmillan Col, New York, 1965.

25. P. V. Gray, Paper presented at the Silicon Interface Specialists Conference, March 1-3, 1967, Los Vegas, Nev.